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The Open Automation and Control Systems Journal, 2014, *6*, 1451-1455

A Compiler Design Technique for EMS Test CS115

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Abstract: A novel method using software programming to resolve CS115 problems is proposed in this paper. Conductive sensitivity test of CS115 and its effect on the electronic system are shown and discussed. The novelty of this method is using software programming other than hardware-level techniques to resolve CS115 problems which is an important issue in electro-magnetic compatibility. The feasibility of this method is verified by actual tests.

Keywords: Electro-magnetic compatibility(EMC), electro-magnetic compatibility test, CS115, electromagnetic sensitivity.

1. INTODUCTION

Electromagnet compatibility (EMC) problems are a study considering the side effects of a circuit. Digital IC-EMC can be considered as a new branch of EMC research (a computer science-related EMC problem). Various EMC tests are needed based on the actual work environment of the devices. EMC tests include electromagnetic interference (EMI) and electromagnetic sensitivity (EMS) measurements, which is introduced in detail in [1]. EMS tests are divided into Conducted susceptibility (CS) measurements and radiation sensitivity (RS) measurements. The test of CS115 belongs to CS measurements which is important in EMS field. The failing of test CS115 will cause the equipment to work wrong.

To solve this problem, many techniques are proposed. Most of them are based on hardware-level EMS protection techniques [2-4]. The protection of EMS test problems by hardware-level techniques should be done as much as possible.

However, in some cases, updating or upgrading hardware components for such enduring machines is not easy due to many issues. Thus, software-level EMS techniques are alternatives in these cases. The method using software compiler to optimize EMI problems is introduced in [5], but there is seldom paper on software compiler to solve EMS problems.

This paper proposes a software-level method by a compiler technique to solve EMS problem. A communication device can't work properly under CS115 trials are solved using this method. Meanwhile, the interference produced from EMC test of CS115 could also be reduced by this method. This study is not a research on compiler technology but an adaption of computer science-domain technology into EMS optimization research.

This paper is to introduce a new method, using a compiler design method by changing the programming of the device rather than hardware, to solve the problems caused by EMC test of CS115 and meets the EMS test index.

2. CS115 TEST AND ITS AFFECT

CS115 is a CS EMC test whose signal injected into cables, which is used to test the equipment ability that withstanding the effects of coupling to the relevant cables from fast rising-and-falling (RAF) transient currents. The repetition frequency of standard test signal waveform is 30Hz, and the rise time is 2ns, and the pulse width of a signal is last 30ns. This transient current may be due to the switching operation of the platform, lightning, electromagnetic pulses and other external transient environmental factors.

One pulse waveform of CS115 in time domain is shown in Fig. (**1**), the range of the pulse is 250V by GJB151A standard. The high-frequency spectrum of the pulse depends on the trapezoidal pulse RAF time. The shorter the RAF time, the higher frequency spectrums are produced. Generally, 2 ns RAF time can produce a bandwidth of approximately 160 MHz noise. The frequency domain waveform is shown in Fig. (**2**), which is transformed by FFT of the pulse shown as Fig. (**1**).

The test CS115 is CS measurement which is used to check if the EUT can tolerate the interference signal level invaded by the cables. As shown in Fig. (**1**) and Fig. (**2**), in our test, the interference signal repeat at 30Hz, the RAF time of the signal is 2ns, the pulse width is 30ns and the frequency bandwidth is 160 MHz

The signal received above is the source of interference testing of CS115, whose interference signals conducted into the interior of the device through cables. The electronic device connected to the cable bundle is sensitive equipment. The CS115 test whose interference conducted into the internal device *via* cables may cause the device working

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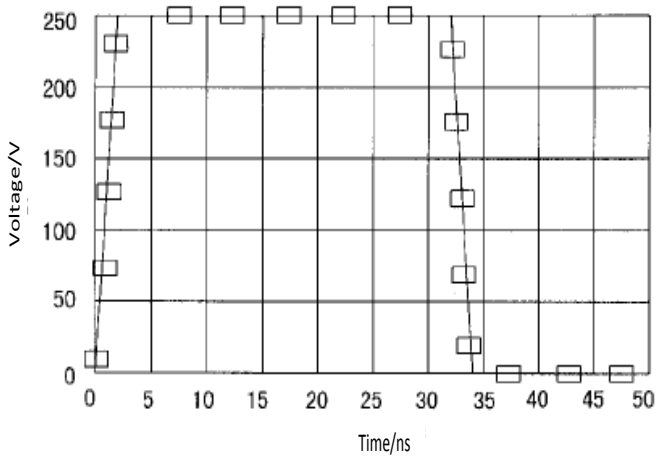

Fig. (1). Time domain of CS115.

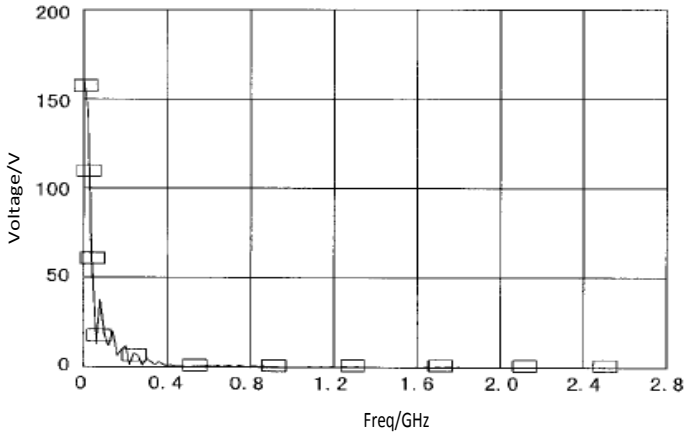

Fig. (2). Frequency formation of CS115.

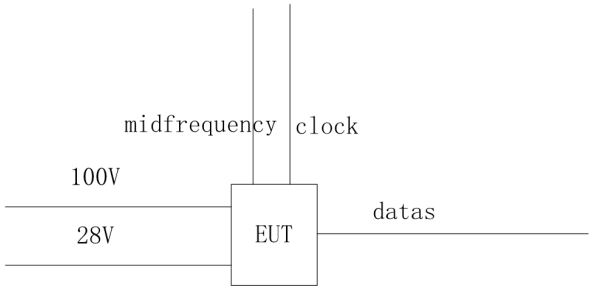

Fig. (3). CS115 test diagram.

improperly. Impact of rising / falling edge brings wideband noise and transient disturbances and must be taken into account in this test. Generally, shielded cable or port added filtering can protect the effects of such interference.

However, even if the device is shielded, etc., effect from CS115 test is still to be considered. The noise caused by CS115 interference will increase a lot, which will result in a digital circuit level conversion errors and device or system function errors.

3. TEST PROBLEMS AND SOLUTIONS

3.1. Test Analysis Problem

The lines of equipment under test (EUT) are shown in Fig. (**3**). When CS115 interference is added to the lines, the test dysfunction will appear only except the 100V line was added the interference. That may be because the lines share the same ground, the noise on the ground is too large and may cause the digital circuit level conversion error.

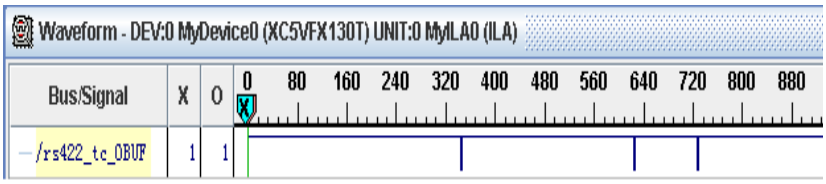

Fig. (4). Interface data interference figure at RS422.

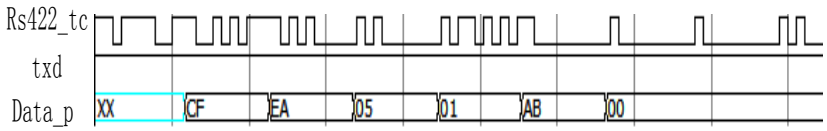

Fig. (5). Normal simulation interface data of RS422.

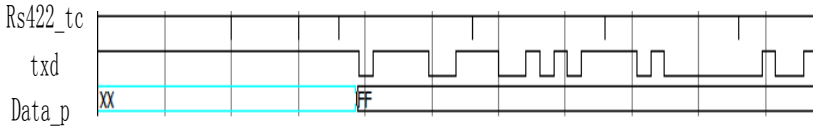

Fig. (6). Anomal simulation interface data of RS422.

Therefore, the preliminary work to determine the equipment noise is necessary when the CS115 interference joins, which had an impact on device functionality.

Note: midfrequency and clock are coaxial; 100V and 28V both are twisted pair, where the ground of 100V is isolation with equipment, and the ground of 28V is common ground with equipment ground; datas cables are shielded twisted pair cables.

In order to further determine the location where the device is affected when CS115 interference is added, using JTAG data cable to download bit files to a FPGA (Hardware Description Language is used in FPGA). In the case of load interference, use ISE Chip Scope software to test transmitting unit and a receiving unit, and we find that the RS422 differential serial data transfer interface is affected shown in Fig. (**4**). Intermittent glitches interference is found in the input data (rs422_tc_OBUF); this phenomenon is consistent with the characteristics of transient interference CS115.

RS422 is a differential serial transmission. When it receives data it can judge the head of data and checksum and it can only returns the correct response with both of the head of data and checksum correct. RS422 data format is defined as follows:

Baud Rate：9600bps

Data bits：8bits

Odd and even parity bit：none

State bit：1bit

Stop bit：1bit

RS422 start bit is a low level one-bit, so it will determine start bit by the falling edge of the data without considering the interference. This is why the interference of Fig. (**4**) is judged to be the start bit improperly.

To further study the effect when interference added, the testing phenomenon is simulated by the software of ModelSim 6.3. As shown in Fig. (**5**), it is normal and correct parse input and output data simulation maps. Fig. (**6**) is abnormal input data (analog CS115 plus interference waveform). In this case, both the output response (txd) and analytical data (data_p) are wrong. Fig. (**6**) shows that the output Data behave wrongly when the normal input data can't be offered. The misjudgment of the interfering signals by the software caused the output data wrong, which also causes the abnormal function in the test.

Note: "rs422_tc" is input data, "txd" is output data, "data_p" is Analytical data.

Note: "rs422_tc"is added interferency, "data_p" is FF.

3.2. Solutions

The comparison of simulation and testing results can proved that the input data interference by CS115 will lead to abnormal function in EMC test. Filtering or shielding in hardware is the conventional way to solve the problems of EMC. Here, we adopt software method to solve the problems mentioned above. We analyze the situation of the input data by interference, and find that the software mistakenly regard

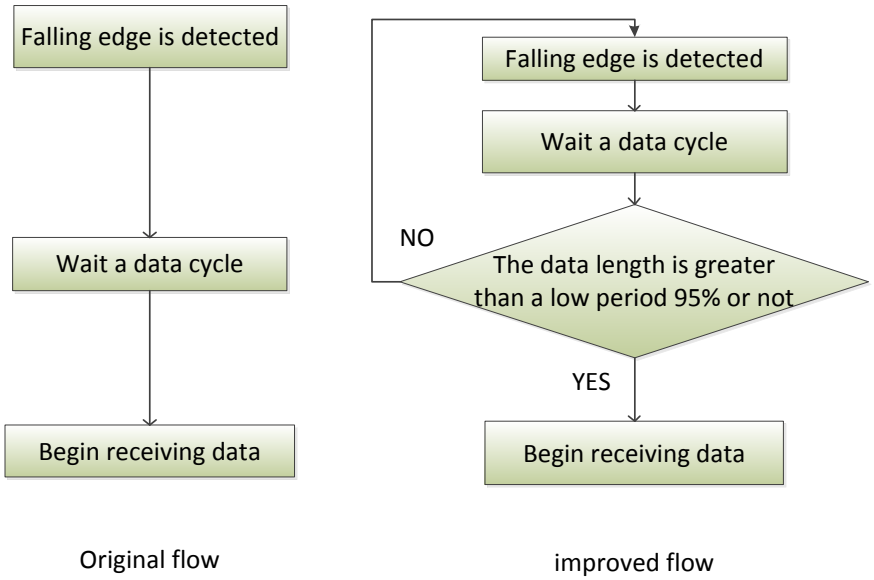

Fig. (7). Change the program flow before and after contrast (fragment).

interference signal of CS115 as a trigger, which results in the generation of the corresponding error. CS115 interference is transient interference, so we increase the length of time judgment sentences in the software, which can exclude the impact of CS115 intelligently on the system. Program changes before and after comparison are shown in Fig. (**7**):

The determining program statement of VHDL is shown as follows:

```
If (counter_fenpin<1041) then
 counter_fenpin<=counter_fenpin+1;
 if(rs422_tc_gg='0') then
 leiji<=leiji+1;
 end if;
else
 if (leiji>990) then
 n_state<="10";
 counter_fenpin<=(others=>'0');
            leiji<=(others=>'0');
    else
            n_state<="00";
        leiji<=(others=>'0');
    end if;
end if;
```

The baud rate of RS422 is 9600bps, and the clock is 10M, so the clock number that a data width occupied is

$$\frac{10*10^6}{9600} \approx 1041 \quad (1)$$

After the arrival of first falling it needs about 1041 clock cycles, and during this period RS422 data on low-level is accumulated. The length should be less than the width of a data (Determine program uses 95 percent is a reasonable width of the data), that is:

$$1041*0.95 = 988.95 \quad (2)$$

Procedures for judging rounded to 990, which is enough to determine the interference caused by the CS115, is not a reasonable start bit time, so the effect of interference can be avoided by the device function determination program.

3.3. Verification:

The program is simulated by ModelSim 6.3 software. As shown in Fig. (**8**). The output data is correct after software process. The results of Fig. (**8**) are compared with the results of Fig. (**6**), with the same CS115 interfering signal injecting to the equipment, and we can see that the equipment added the statement is not affected by the presence of disturbance signal.

The VHDL program that is added a judgment statement is used in the actual EMC test and the test can be passed, which can further prove that the program is proper and effective.

CONCLUSION

In this paper, we have proposed a novel software technique to solve the side effect of EMC test CS115. For any EMS problems, various hardware-level techniques should first be adapted as much as possible. However, component upgrading for an enduring machine is sometimes not easy. Thus, software-level EMS solution techniques are useful alternatives.

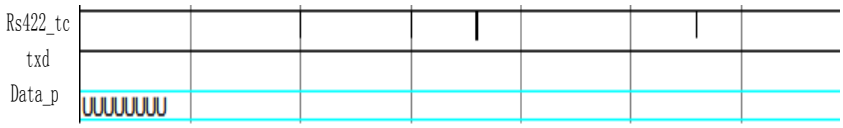

Fig. (8). Normal simulation interface data of RS422.

This paper adapts compiler technology into the EMS problem. According to the theory of compiler and the proposed EMS procedure, we design a process adding a judgment. The judgment can decide which signal is interference and avoid the interference affecting the function of device. According to the simulation and measurement results, the compiler is verified effective.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

Declared none.

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Received: September 16, 2014 Revised: December 23, 2014 Accepted: December 31, 2014