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An Adaptive Length Frame Synchronization Scheme

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Abstract: In order to improve the frame synchronization performance of the adaptive length frame transmission system, a frame synchronization scheme is proposed. The scheme considers the false loss probability relating to the bit error rate and the false alarm probability relating to the model of synchronous header are considered synthetically. Then the performance formulas of general frame synchronization are given and analyzed to obtain the relevant frame synchronization parameters. In the end, based on the frame synchronization parameters, the scheme performance of adaptive length frame synchronization is simulated. The simulations show the adaptive length frame transmission system can realize frame synchronization effectively.

Keywords: Adaptive length frame, frame synchronization header, frame synchronization, performance parameters, reliability, *Z* transform.

1. INTRODUCTION

The reliability for backside data disposal and the whole performance of a communications system are insured by the technique of frame synchronization by checking the frame synchronization mark and picking up the frame data [1, 2], [3]. The technique of frame synchronization has gained considerable attention in theory and application, such as the selecting standard for synchronization header model [4, 5], the searching arithmetic for synchronous header [6, 7], design of appointed frame synchronization system [8-10], and so on.

The technique of adaptive length frame transmission can increase the throughput to a certain extent and add the difficulty of frame synchronization [11-13]. Aiming at the difficulty for identifying the adaptive length frames, a frame synchronization scheme for adaptive length frame transmission system is researched to realize the frame synchronization adequately and ensure the reliability of data transmitting and processing. In this scheme, the probability of false loss relating to the bit error rate and the probability of false alarm relating to the model of synchronization header are considered synthetically. Then the performance formulas of general frame synchronization are given and analyzed to obtain the relevant frame synchronization parameters. Finally, based on the frame synchronization parameters, the performance of this scheme is simulated. Simulations show this scheme can realize frame synchronization of the adaptive frame length system effectively and ensure the reliability of data transmission and processing.

2. RESEARCH ON FRAME SYNCHRONIZATION SCHEME

The serial data uses a frame to be a discriminating unit. At frame start is laid a Frame Synchronization Header (FSH) with the excellent relativity. The Frame Length Marker (FLM) is placed between the FSH and the frame. The length of FSH, FLM and frame are N, N_{fm} and N_f bits respectively.

In the frame synchronization Searching States (SS), the frame synchronization system analyses the FSH bit by bit.

Once the FSH is analyzed, the frame synchronization system enters the frame synchronization Checking States (CS). In the CS, system reads the frame length information in the FLM and checks the next FSH. If checking another FSH before the next frame, the previous FSH will be discarded. Secondly, system checks the FSH until the next frame start. If the FSH is not checked in this course, the previous FSH will be considered as a false FSH or some error bits are in the FLM, then system returns the SS. Otherwise, in the CS, if checking $a-1$ FSHs continuously, system enters the frame synchronization Locking States (LS) and begins to deal with frame data.

After entering the LS, the frame synchronization system needs to still check the FSH. If the false FSH is not checked in the frame synchronization locking and holding process, the system will enter the frame synchronization Holding States (HS)

In HS, system reads the FLM and checks the FSH of the next frame. If there are error bits in the FLM, the system will pick up the frame length information N_f based on the seriate of two FSHs. Losing the continuous b-1 FSHs or once checking the false FSH, system will stop taking count of holding frame synchronization and enter the SS. Otherwise, system returns to the LS.

So the frame synchronization holding process can be partitioned, the frame synchronization holding process I(HS-I) arose by bit error in the FLM and the FSH and the frame synchronization holding process II(HS-II) arose only by bit error in the FSH. During the HS-I, FSH is real loss. So the time of HS-I and the frame synchronization analyzing and checking process are defined to be the frame synchronization

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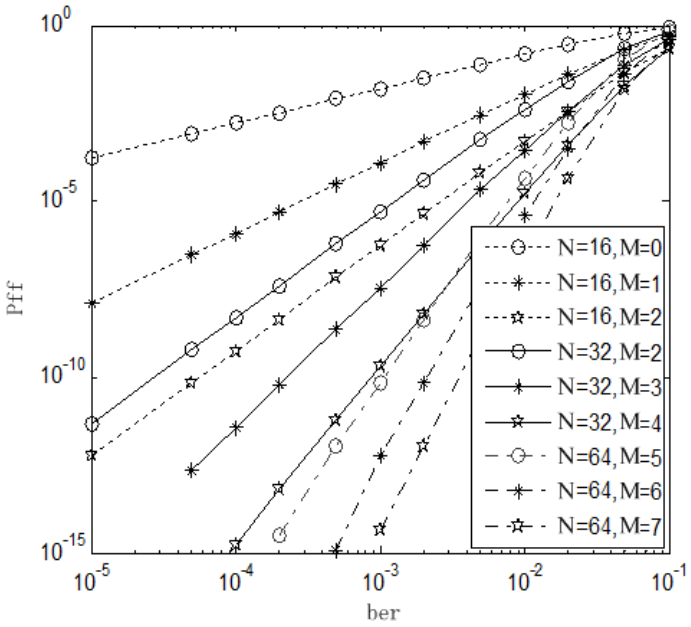

Fig. (1). Relation of P_{fm}, *ber* and N_{fm}.

loss time. During the HS-II, the FSH is unreal loss. So the time of HS-II is defined as the frame synchronization duration time.

3. PERFORMANCE ANALYSIS OF FRAME SYNCHRONIZATION SCHEME

The probability of checking a false FSH, and the probabilities of including error bits in the FLM or FSH are defined as

$$P_{ff} = 0.5^N \sum_{i=0}^{M} C_N^i \tag{1}$$

$$P_{fm} = 1-(1-ber)^{N_{fm}} \tag{2}$$

$$P_h = 1-\sum_{i=0}^{M} C_N^i (1-ber)^{N-i} ber^i \tag{3}$$

Where, M bits is the bounds of admitting bit error in the FSH, and *ber* is the bit error rate in channel.

The best frame synchronization code type is shown as Table **1**.

When N_f=8192 bits, the P_{ff} is shown as (Fig. **1**).

Table 1. The best frame synchronization code type.

N (bits)	code type
8	B8
16	EB90
32	1ACFFC1D
64	FFF2D58B65466000

As shown as (Fig. **1**), P_{ff} has relation to M and N but has no relation with *ber*. If M or N is larger then P_{ff} is smaller. When N=32 bits (namely, the frame synchronization code type is EB90) and M<3 bits, $P_{ff} \rightarrow 10^{-7}$.

When N=32 bits and N_f=8192 bits, the P_{fm} and P_h are shown as (Fig. **2**) and (Fig. **3**).

(Fig. **2**) shows that P_{fm} has relation to *ber* and N_{fm} but not with M. If *ber* or N_{fm} is larger then P_{fm} is bigger. N_{fm} =k bits can denote 2^k frame length.

(Fig. **3**) shows that P_h has relation to *ber* and M. If *ber* is larger or M is smaller then P_h is bigger. Let M=2 bits, when *ber*<10^{-2}, $P_h \approx 0$.

The probability of researching the true FSH in a frame is

$$P_1 = \frac{1-P_h}{N_f} + \frac{1-P_h}{N_f}(1-P_{ff}) + \ldots + \frac{1-P_h}{N_f}(1-P_{ff})^{N_f-1}$$

$$= \frac{(1-P_h)\sum_{k=1}^{N_f}(1-P_{ff})^{k-1}}{N_f} \tag{4}$$

Let P=(1－P_h)(1－P_{fm}), then the states of system entering LS transfer is shown as Fig. (**4**).

The Z switch is shown as follows separately.

$$SS(Z) = \frac{P_1 Z^N}{1-(1-P_1)Z^N} \tag{5}$$

$$CS_1(Z) = \frac{PZ^N}{1-SS(Z)(1-P)Z^N} \tag{6}$$

$$CS_2(Z) = \frac{PZ^N}{1-SS(Z)CS_1(Z)(1-P)Z^N} \tag{7}$$

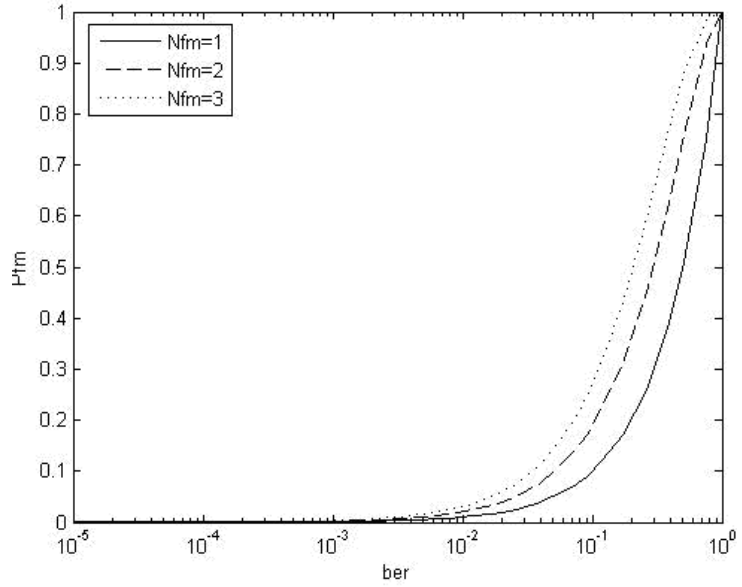

Fig. (2). Relation of P_{fm}, *ber* and N_{fm}.

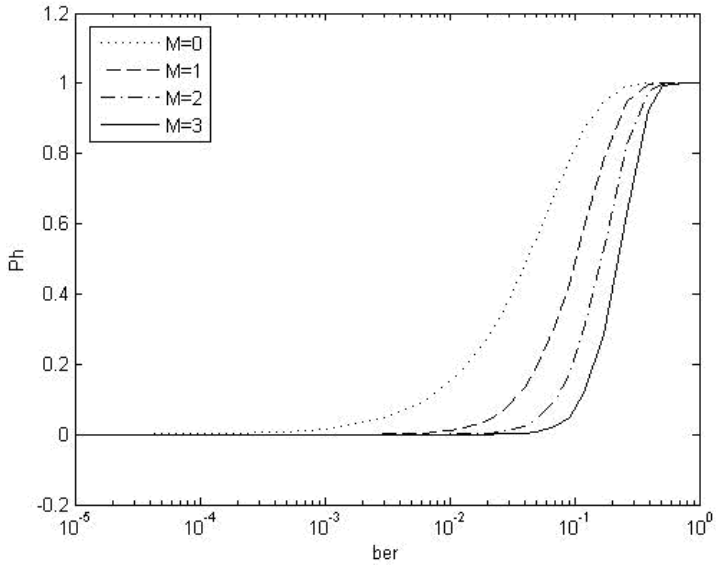

Fig. (3). Relation of P_h, *ber* and *M*.

So when i =2,…,a-1, $CS_i(Z)$ is shown as follow.

$$CS_i(Z) = \frac{PZ^N}{1 - SS(Z)\prod_{j=1}^{i-1} CS_j(Z)(1-P)Z^N} \tag{8}$$

Then the unitary time of the system entering LS can be given as

$$T_{ELS} = \frac{1}{N}\left[\frac{d(SS(Z)\prod_{i=1}^{a-1} CS_i(Z))}{dZ}\right]\Bigg|_{Z=1}$$

$$= \frac{(1 + P_1 - P - P_1 P^{a-1})}{P_1(1-P)P^{a-1}} \tag{9}$$

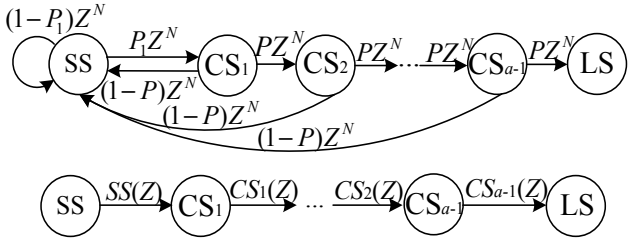

Fig. (4). States transfering of LS.

The states of system entering the HS-I is shown as Fig. (**5**).

So, we can get the Z switch for system entering the HS-I state as (10).

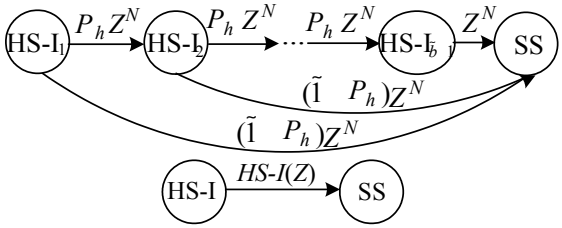

Fig. (5). States transferring of HS-I.

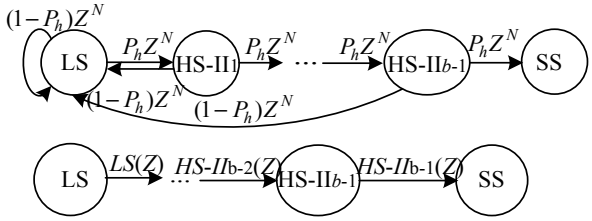

Fig. (6). States transferring of HS-II.

$$HS-I(Z)=(1-P_h)Z^N\sum_{m=0}^{b-3}(P_hZ^N)^m+(P_hZ^N)^{b-2}Z^N \tag{10}$$

The states of system entering the HS-II are shown as Fig. (**6**).

Then, we can get the Z switch for system entering the HS-II state as follows.

$$LS(Z)=\frac{P_hZ^N}{1-(1-P_h)Z^N} \tag{11}$$

$$HS-II_1(Z)=\frac{P_hZ^N}{1-LS(Z)(1-P_h)Z^N} \tag{12}$$

$$HS-II_2(Z)=\frac{P_hZ^N}{1-LS(Z)HS-II_1(Z)(1-P_h)Z^N} \tag{13}$$

So when i =2,…,b-1, $HS-II_i(Z)$ is shown as follows.

$$HS-II_i(Z)=\frac{P_hZ^N}{1-LS(Z)\prod_{j=1}^{i-1}HS-II_j(Z)(1-P_h)Z^N} \tag{14}$$

The unitary time of entering HS-I is

$$T_{HS-I}=\frac{(1-P_h^{b-1})}{(1-P_h)} \tag{15}$$

The time of frame synchronization loss arose by bit error in the FLM and FSH is

$$T_{L1}=P_{fm}P_h(1+T_{HS-I})$$

$$=\frac{(1-P_h^{b-1})P_{fm}P_h}{(1-P_h)} \tag{16}$$

So the time of synchronization loss is

$$T_L=T_{L1}+T_{ELS} \tag{17}$$

The time of synchronization duration is

$$T_H=\frac{(1-P_h^b)}{(1-P_h)P_h^b} \tag{18}$$

4. PERFORMANCE SIMULATION OF FRAME SYNCHRONIZATION SCHEME

Letting M=2, N=8000 and N_{fm}=1 bits, the numerical simulation of frame synchronization performances for adaptive frame length system are shown as (Fig. **7**) and (Fig. **8**).

Fig. (**7**) shows that T_L is small at lower *ber*, but large at higher *ber*. When *ber*$\leq 10^{-2}$, $T_L\approx 0$ no matter what values b and a are. And if a is greater, then T_L increases faster. Be-

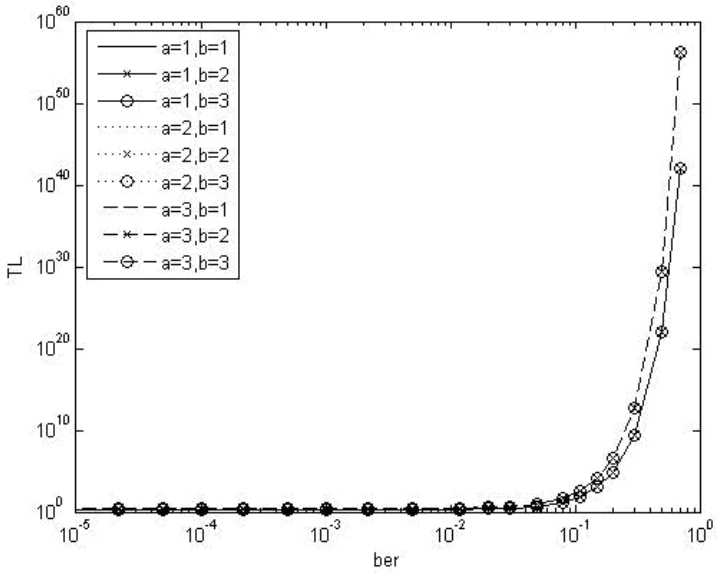

Fig. (7). The curve of T_L.

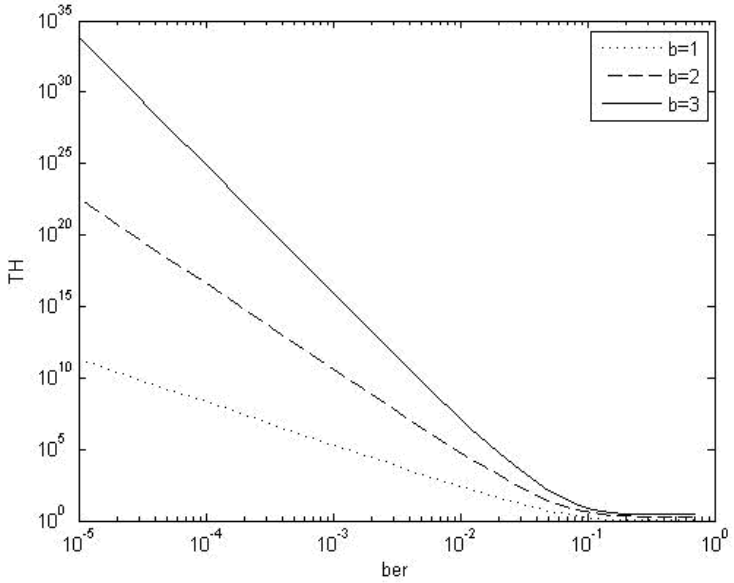

Fig. (8). The curve of T_H.

cause, during searching FSH bit by bit and checking FSH frame by frame, the increase of *ber* and *a* leads FSH and FLH to be leaked frequently. So T_L is prolonged. When the channel condition is good (namely *ber* is smaller), T_L is only related to *a* (T_L=*a*). Therefore, for decreasing T_{EL}, the smaller *a* should be taken. So making *a*=2 can ensure the reliability of LS.

Fig. (**8**) shows that T_H is large at lower *ber*, but is small at higher *ber*. Obviously, when channel condition is good, P_{fm} and P_h are low and $P_h << P_{fm}$. System will keep in HS-II. And *b* is larger, the time in HS-II is longer. Then T_H is larger. When channel condition is bad, FSH will be lost frequently and T_H is small. To improve T_H, the larger value of *b* should be taken. But, the length of frame is not fixed in frame length adaptive system. Once losing FSH for FLH error, system will lose all data contained in the frame. Therefore, to increase data reliability, *b* should not be too large. So making *b*=2 can enhance T_H .

Table 2. Error lock probability.

	***a*=1**	***a*=2**	***a*=3**	***a*=4**
M=16	2.0×10^{-4}	5.9×10^{-8}	1.1×10^{-11}	3.0×10^{-15}
M=32	6.7×10^{-9}	8.5×10^{-15}	1.1×10^{-20}	1.4×10^{-26}
M=64	6.0×10^{-18}	2.3×10^{-28}	8.7×10^{-39}	3.3×10^{-49}

Table 3. Unlock probability of after error lock.

	b=1	**b=2**	**b=3**	**b=4**
M=16	0.9997	0.9995	0.9992	0.9989
M=32	0.99998	0.99997	0.99997	0.99994
M=64	0.99999999996	0.99999999992	0.99999999988	0.99999999984

Under different parameters, the simulation results about the probability of frame synchronization error lock are shown as Table **2**.

Under different parameters, the simulation results about the probabilities of frame synchronization unlock after error lock are shown as Table **3**.

According to the results of Table **2** and Table **3**, the values of frame synchronization parameter can be advice as Table **4**.

When *a*=*b*=2, the simulation results of throughput in the adaptive frame length scheme and the fixed frame length scheme are shown as (Fig. **9**).

As a whole, the throughput of adaptive scheme is superior to the fixed scheme obviously.

CONCLUSION

The time of frame synchronization loss T_L and the time of frame synchronization duration T_H are important performance parameters to frame synchronization scheme. The good frame synchronization scheme must make T_L short but T_H long. From the performance formulas of this scheme, the relevant frame synchronization parameters can be obtained. Based on those, the frame synchronization performances of adaptive frame length system are simulated. Simulations show when *a*=*b*=2 this scheme can realize adaptive length

Table 4. Advice values of frame synchronization parameter.

	M	**a**	**b**
N=16	1	≥3	≥3
N=32	2	2 or 1	2 or 3
N=64	5	1	2 or 1

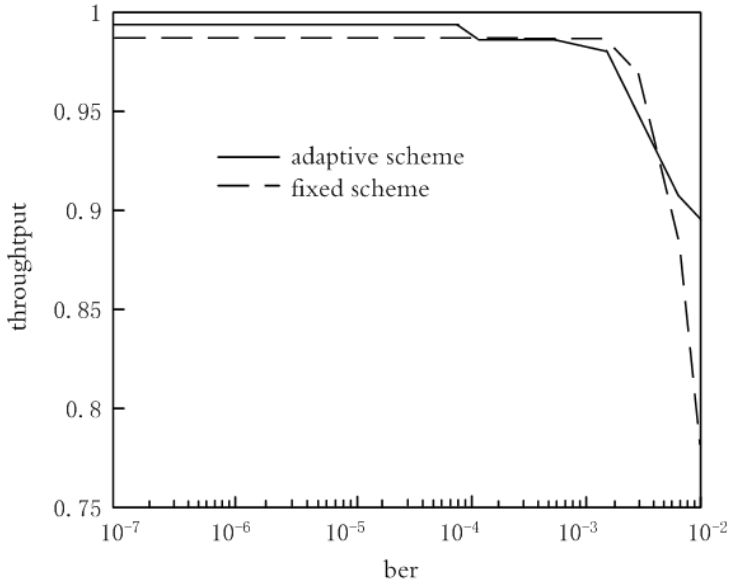

Fig. (9). The curve of throughtput.

frame synchronization effectively and ensure the reliability of data transmission and processing for the adaptive length frame transmission system. Simulations show that the proposed scheme is suitable for the adaptive frame length system adequately and the system outstanding throughput can be ensured effectively. So the new scheme presented in the paper is valid.

CONFLICT OF INTEREST

The author confirms that this article content has no conflict of interest.

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