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Power-Gating Single-Rail MOS Current-Mode Logic Circuits Using High-Threshold PMOS Transistors as Linear Resistors

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Abstract: In this paper, a power-gating technology for single-rail MOS Current Mode Logic (SRMCML) circuits is presented, which use the high-threshold PMOS transistors as linear load resistors to reduce the power dissipation in the sleep mode. The basic SRMCML cells, such as buffer/inverter, AND2/NAND2, AND3/NAND3, OR2/NOR2, OR3/NOR3, XOR2/XNOR2, multiplexer, and 1-bit full adder, are used to verify the effectiveness of the proposed power-gating scheme. The equivalent model for calculating energy dissipations of the power-gating SRMCML circuits is constructed. All circuits are simulated with HSPICE at a 130 nm CMOS process. By simulating power-gating SRMCML circuits in active and sleep modes, it is concluded that the power dissipation of power-gating SRMCML circuits in sleep mode is reduced with the decrease of the device sizes of high-threshold PMOS sleep transistors, while the power dissipation of power-gating SRMCML circuits is almost independent of the device sizes of sleep transistors in active mode. The power dissipation comparisons among power-gating SRMCML, conventional SRMCML, and power-gating static CMOS circuits are carried out. The power dissipation of the proposed power-gating SRMCML circuits is the least among the three above mentioned structures.

Keywords: Energy-efficient design, high-speed digital circuit, modeling optimizing of sleep transistors, MOS current mode logic, power-gating technology.

1. INTRODUCTION

MOS current mode logic (MCML) can operate in a higher frequency than conventional CMOS logic due to its small output voltage swings [1-6]. Its high-speed applications such as high-speed processors and Gps multiplexers for optical transceivers have been widely addressed [5, 6]. MCML circuits are usually realized with the dual-rail scheme using a NMOS pull-down network (PDN) and its complementary NMOS PDN, which is similar to evaluation tree in DCVSL (Differential Cascode Voltage Switch Logic) [7]. The dual-rail MCML (DRMCML) circuits increase extra area overhead and the complexity of the layout place and route. Currently, single-rail MCML (SRMCML) circuits have been reported [8]. SRMCML are realized by only using a signal NMOS pull-down network, and thus reduce the transistor counts of a logic gate and the complexity of the layout place and route.

The power consumption of both DRMCML and SRMCML circuits is proportional to its supply voltage and bias current because of constant operating current. Therefore, the power consumption of a MCML gate is constant in spite of its operating frequencies and activities of input signals [9, 10]. This means that the static power consumption of MCML cells is significantly higher than equivalent implementations using conventional static CMOS logic [11, 12].

With the growing uses of portable and wireless electronic systems, both low-power and high-speed designs have become increasingly common and important. Because not all function blocks or modules in a system are in active mode, the leakage dissipations of conventional CMOS circuits in sleep mode can effectively reduce by introducing multi-threshold CMOS (MTCMOS) power-gating technologies. In conventional CMOS circuits, power-gating circuit uses usually high-threshold devices as sleep transistors to reduce their leakage power dissipation [13]. Similarly, idle MCML logic blocks can be also shut down by using power-gating switches to reduce their standby power dissipations.

Several power-gating schemes for MCML circuits have been proposed to reduce the power dissipation in sleep mode [14, 15]. Cevrero *et al.* proposed a power-gating scheme by inserting NMOS sleep transistors between the power-gated MCML block and ground. The results shows that static power consumption is significantly reduced with a delay penalty of 2.7% and area overhead of about 5.6% for basic logic cells such as AND/NAND and multiplexer gates [14]. Kim used an additional PMOS high-threshold transistor that is inserted in series between the supply voltage and the MCML cell effectively to reduce the leakage current with a 3% increase in propagation delay and area penalty from 3% - 24.2% for different power-gated function blocks [15]. However, the previously reported power-gating approaches are all investigated for the dual-rail MCML circuits. Moreover, modeling, analyzing, and optimizing methods on the power-gating switches should be also addressed.

In this work, we propose a power-gating scheme for SRMCML circuits. The load PMOS transistors in MCML

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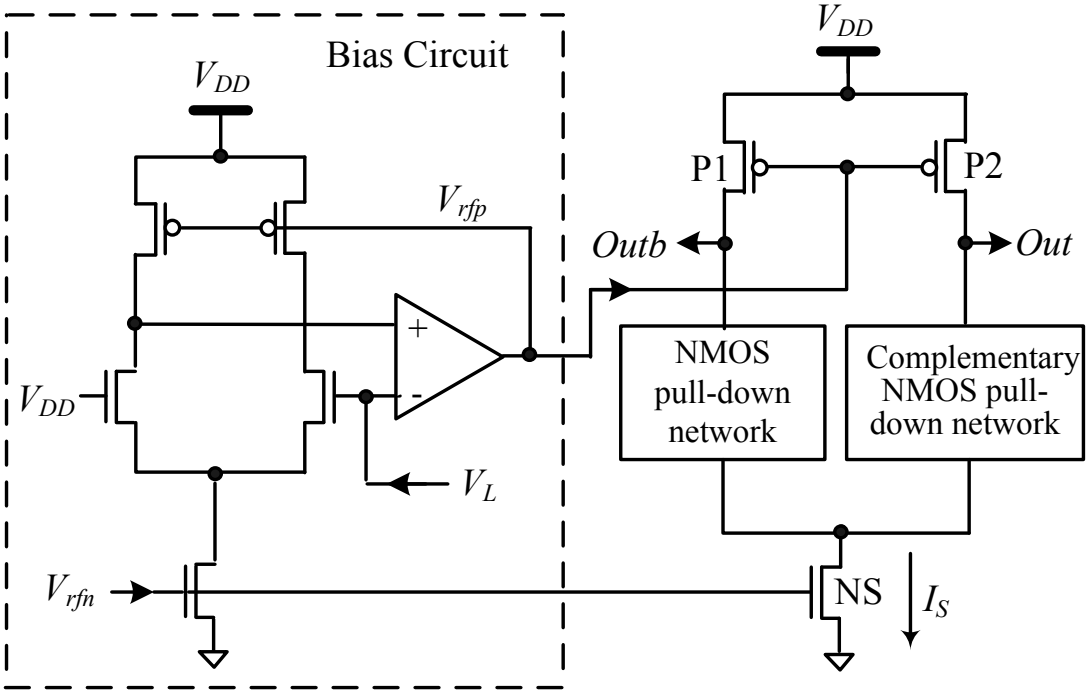


Fig. (1). MCML with dual-rail scheme.

circuits are set as high-threshold devices to reduce the sleep power dissipation. The equivalent model for calculating energy dissipations of the power-gating SRMCML circuits is constructed. The optimization methods for sizing power-gating transistors are addressed in term of power. The proposed power-gating scheme has not additional propagation delay and area overhead.

This paper is organized as follows. In section 2, MCML circuits is reviewed, and the design methods of the basic logic cells based on single-rail MCML are also presented. The power-gating SRMCML circuits are introduced in section 3. Modeling and optimizing of the power-gating switches are addressed in section 4. The power dissipations of the power-gating switches are also investigated in sleep and active modes in section 4. In section 5, the power dissipations of the basic cell cells and 1-bit adder based on power-gating SRMCML circuits are compared with the power-gating static CMOS logic ones. Finally, current and future developments are summarized in the last section.

2. REVIEW OF MCML CIRCUITS

The buffer/inverter based on conventional dual-rail MOS Current Mode Logic (DRMCML) and its biasing circuit are shown in Fig. (**1**). The DRMCML buffer/inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull-down switch network consisting of the NMOS pull-down network (PDN) and its complementary NMOS PDN, and the current source transistor (NS). The load transistors are designed to operate at linear region with the help of the control voltage V_{rfp} produced by the bias circuit, which also control the output logic swings. The signal V_{rfn} is used to control the demanded bias current I_S, which is mirrored from the current source in the bias circuit.

DRMCML circuit is a differential logic one with dual-terminal input and dual-terminal output ports like DCVSL [7, 16]. This structure results in extra area overhead, because the two complementary PDNs must be used. Moreover, the dual-rail structure increases complexity of the layout place and route. Recently, single-rail MCML (SRMCML) circuits were proposed, as shown in Fig. (**2**) [8].

The SRMCML circuits are realized only using a NMOS pull-down network to perform the demanded logic operation. The complementary NMOS PDN used in the DRMCML circuit is replaced with a NMOS transistor, and its output is fed back the gate of this NMOS transistor.

The operation of both DRMCML and SRMCML circuits is performed in the current domain. The pull-down network switches the constant current between the two branches. The two PMOS load transistors convert the constant biasing current to output voltage swings. The high and low voltages of the outputs (*Out* and *Outb*) are

$$V_{OH} = V_{DD} \tag{1}$$

$$V_{OL} = V_{DD} - I_S R_D \tag{2}$$

where V_{DD} is source voltage, and I_S is bias current of the MCML circuit, and R_D is the linear resistance of the PMOS transistors, respectively. The logic swing of the output voltage can be written as

$$\Delta V = V_{OH} - V_{OL} = I_S R_D \tag{3}$$

The proper logic swing ΔV is obtained by setting the negative-terminal voltage of the operational amplifier in the bias circuit as $V_L = V_{DD} - \Delta V$, as shown in Fig. (**1**) and Fig. (**2**). From Equation (3), for given ΔV and I_S, the linear resistance of the PMOS transistors is determined. The feedback in the

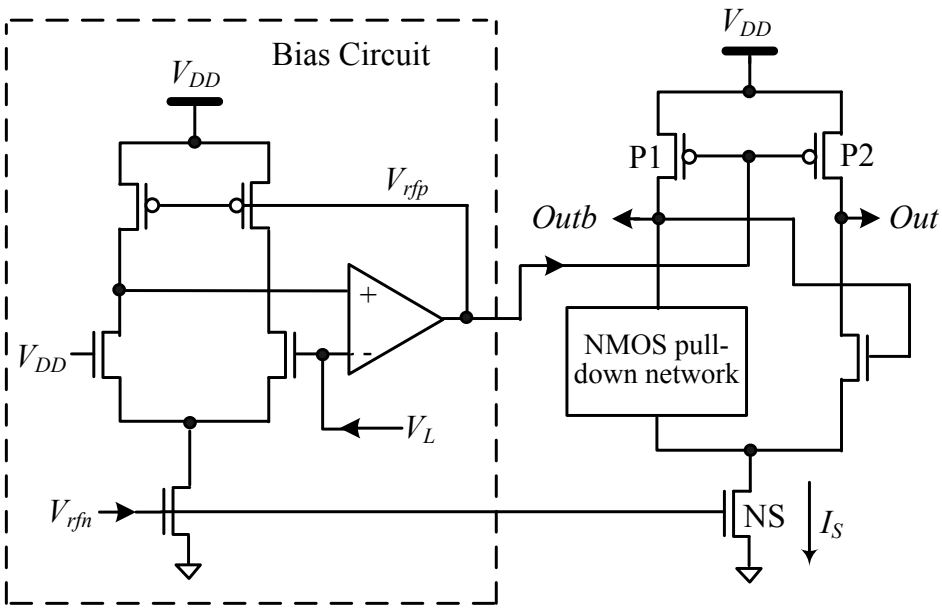


Fig. (2). Single-rail MCML.

bias circuits generates the proper signal V_{rfp} to ensure that the resistance R_D meets Equation (3).

The basic SRMCML gates, such as two-input AND/NAND (AND2/NAND2), three-input (AND3/NAND3), two-input OR/NOR (OR2/NOR2), three-input OR/NOR (OR3/NOR3), XOR2/XNOR2, multiplexer (MUX-21), and two-input XOR/XNOR (XOR2/XNOR2), are shown in Fig. (**3**). As can be seen from Fig. (**3**), the structure of the single-rail MCML circuits is simpler than the dual-rail ones, because only a PDN is demanded. Therefore, the single-rail logic circuits reduce area overhead.

The power dissipation of both DRMCML and SRMCML gates is independent of the switching frequency, and it can been written as

$$P = V_{DD} \cdot I_S \tag{4}$$

From Equation (4), the power dissipation of MCML cells is a constant value for given V_{DD} and I_S.

3. POWER-GATING SCKEMES

The basic structure of power-gating scheme for SRMCML is shown in Fig. (**4**). The power-gating SRMCML circuits are composed of the power-gated logic function blocks, power-gating control circuits, and a bias circuit. In the power-gated logic function blocks, the load PMOS transistors are set as high-threshold devices to reduce the power dissipation in the sleep mode, which is different from the power-gating methods used in [14] and [15], where an additional high-threshold transistor is demanded. Therefore, the proposed power-gating scheme does not demand additional transistors.

In Fig. (**4**), the power-gating control circuits that consist of the PMOS transistor PG1-PGN and the NMOS transistor NG1-NGN are used to switch the high-threshold PMOS transistors under the control of the signal Sleep1b – SleepNb. In power-gating circuits, not all function blocks are shut down at the same time. Therefore, in the proposed power-gating scheme, the power-gated blocks can be severally power-gated by introducing several signals (*Sleep1b* – *SleepNb*).

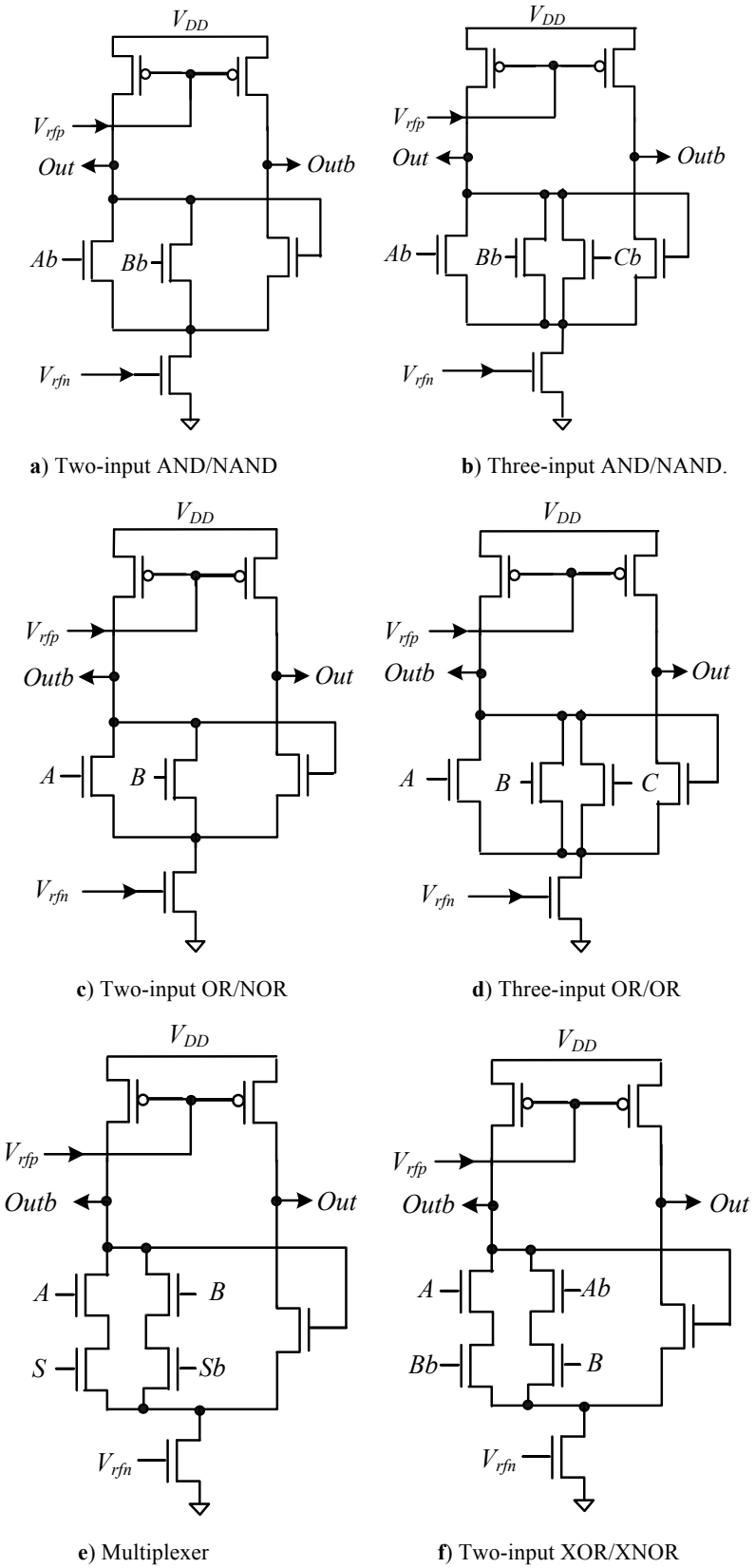
HSPICE simulation waveforms for the power-gating SRMCML OR2/NOR2 gate are illustrated in Fig. (**5**) using SMIC 130 nm CMOS process. By referring the schematics shown in Fig. (**4**) and the waveforms in Fig. (**5**), the operation of the power-gating SRMCML circuits can be summarized as follows:

When the input signal *sleepb* is set as high, NG is turned on and PG is turned off, so that the gate of the high-threshold transistors P1 and P2 is biased toward the voltage V_{rfp}. Therefore, the high-threshold PMOS transistors are turns on as linear resistors, and thus SCMCML circuits works in active mode.

As shown in Fig. (**5**), if the gating input *sleepb* is set to 0 V, NG is turned off and PG is turned on, so that the gate of the high-threshold transistors P1 and P2 is pulled up to the source voltage. The SCMCML logic blocks are shut down, and thus SCMCML circuits operates in sleep mode.

4. MODELING & OPTIMIZING

Power-gating operation shall cause energy overhead, which should be analyzed and optimized. Power-gating operation schedule is shown in Fig. (**6**). In a power-gating period, total energy loss E_{total} includes energy consumption E_{active} in active time T_{active}, energy dissipation E_{sleep} in sleep time T_{sleep}, energy loss E_{on} for turning on the power-gating switches, and energy dissipation E_{OFF} for shutting down the power-gating switches.



a) Two-input AND/NAND

b) Three-input AND/NAND.

c) Two-input OR/NOR

d) Three-input OR/OR

e) Multiplexer

f) Two-input XOR/XNOR

Fig. (3). RMCML basic gates: a) Two-input AND/NAND. b) Three-input AND/NAND. c) Two-input OR/NOR. d) Three-input OR/NOR. e) Multiplexer. f) Two-input XOR/XNOR.

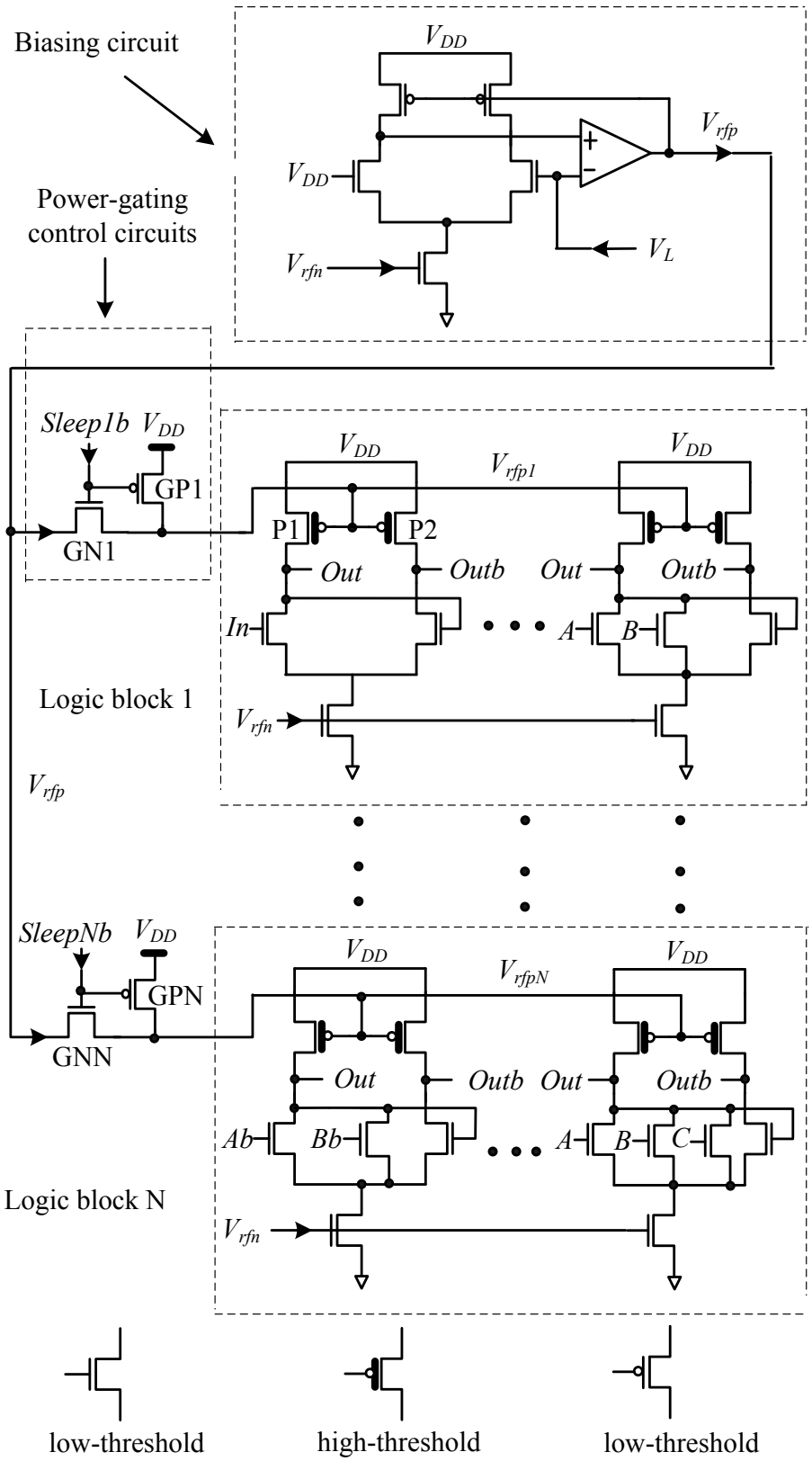


Fig. (4). Power-gating SRMCML circuits.

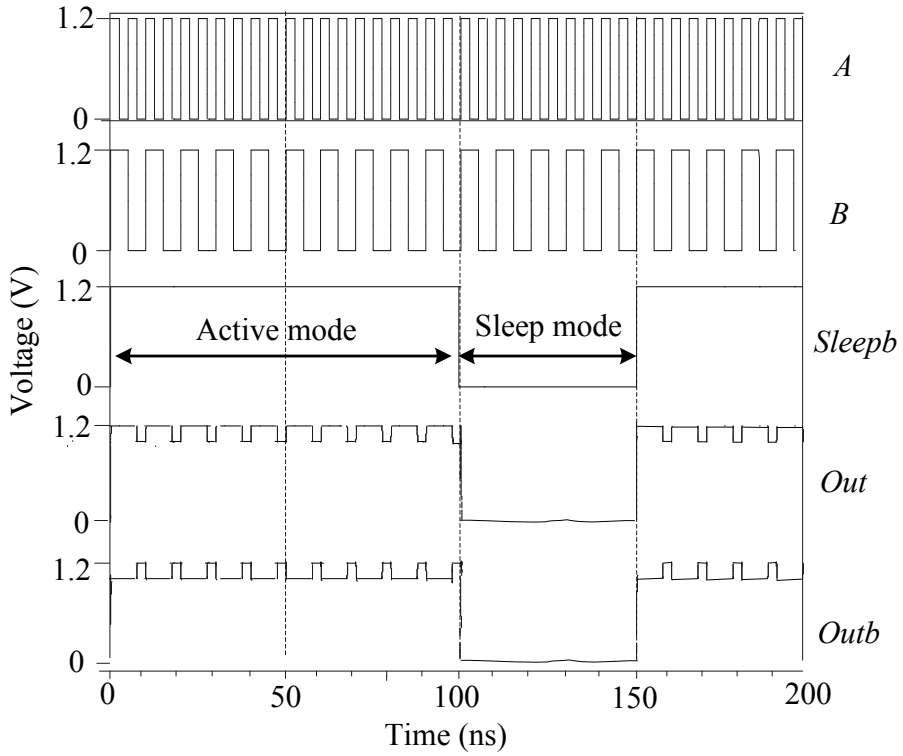


Fig. (5). Simulation waveforms of power-gating SRMCML two-input OR/NOR gate.

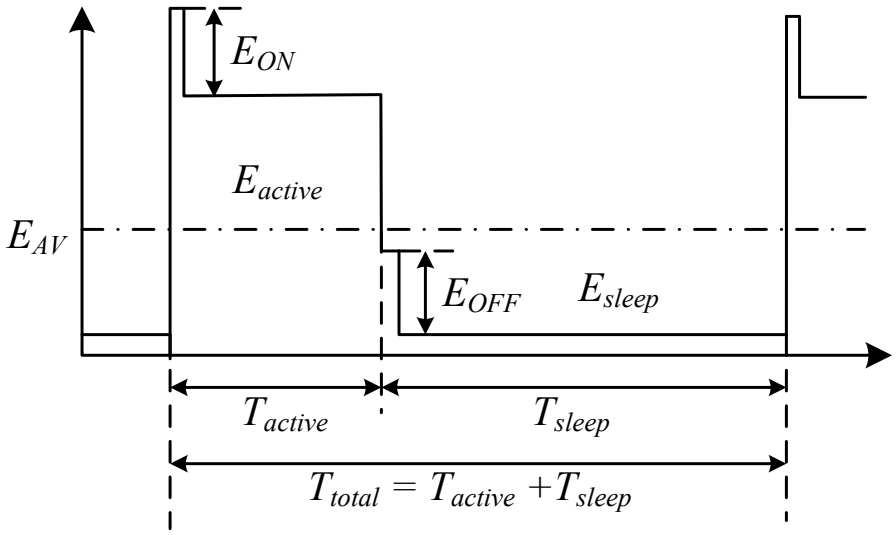


Fig. (6). Power-gating schedule and energy loss.

4.1. Power Dissipation in Active Mode

For the logic block with power-gating switches, the power-gating PMOS transistors (P1 and P2) are turned on during whole active periods. Fig. (**7**) shows the equivalent circuit for calculating the energy dissipation of the power-gating circuits in the active mode. The current that flows through the power source V_{DD} is a constant current I_S. Therefore, the energy loss per power-gating period and power dissipation in active mode are represented as

$$E_{active} = V_{DD} I_S T_{active} \quad (5)$$

$$P_{active} = V_{DD} I_S \quad (6)$$

Fig. (**8**) shows the simulation results for power dissipation of SRMCML buffer/inverter with the different biasing currents in the active mode. In these simulations, the channel length of power-gating PMOS transistors is taken as 0.13 μm, and their minimal channel width (W_{min}) is 0.195 μm. From Fig. (**8**), the power dissipation of SRMCML buffer/inverter

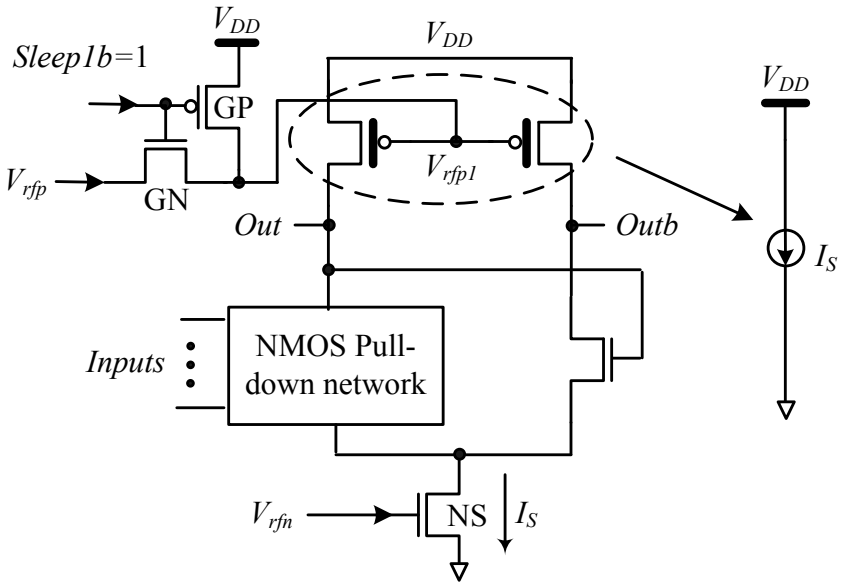


Fig. (7). Equivalent model for calculating energy loss in active mode.

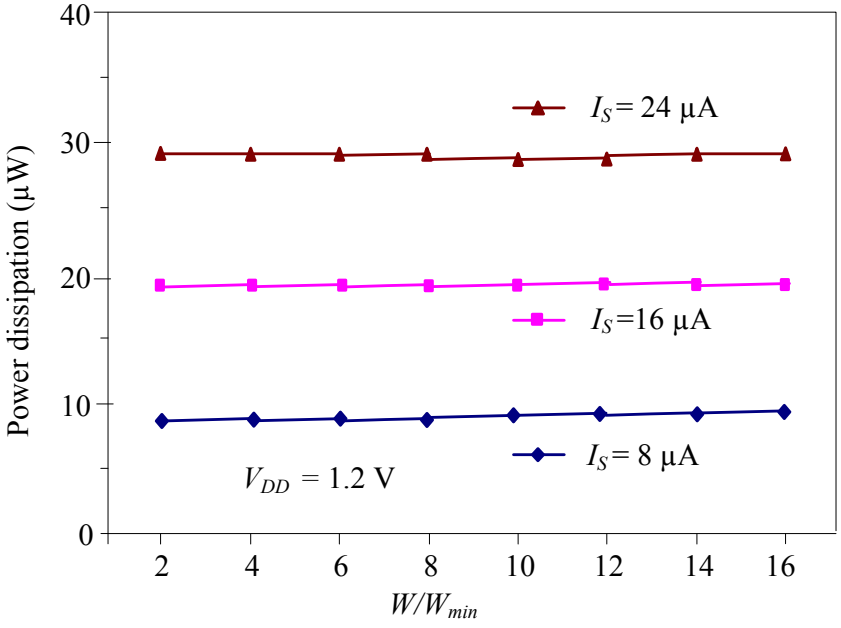


Fig. (8). Power dissipation of power-gating SRMCML buffer/inverter in active mode with different biasing currents. Channel length of power-gating transistors is 0.13 µm, and W_{min} is 0.195 µm.

is independent of the channel width of power-gating transistors, and it is only proportional to biasing current and source voltage.

4.2. Power Dissipation in Sleep Mode

In sleep mode, the power-gating PMOS transistors are turned off, and the SRMCML block is shut down. The current flowing through the power source V_{DD} is only leakage power of the power-gating transistors. The equivalent circuit for calculating the energy dissipation of the power-gating circuits in sleep mode is shown in Fig. (**9**). The energy loss per power-gating period and power dissipation in sleep mode can be written as

$$E_{sleep} = V_{DD} I_S T_{sleep} \tag{7}$$

$$P_{sleep} = V_{DD} I_S \tag{8}$$

Simulation results for the power dissipations of power-gating SRMCML buffer/inverter with the different size of the power-gating transistors in sleep mode are shown in Fig. (**10**). In these simulations, the bias current I_S is set as 16 µA. The channel length of power-gating PMOS transistors is

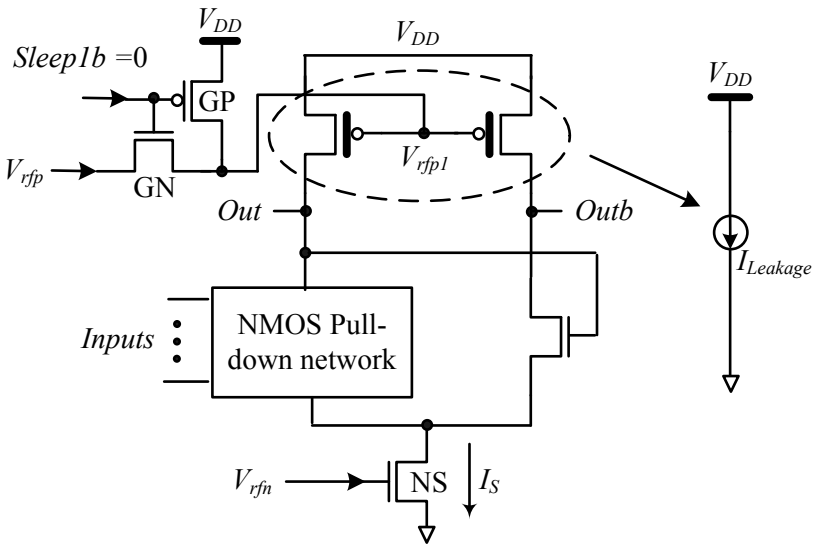


Fig. (9). Equivalent model for calculating energy loss in sleep mode.

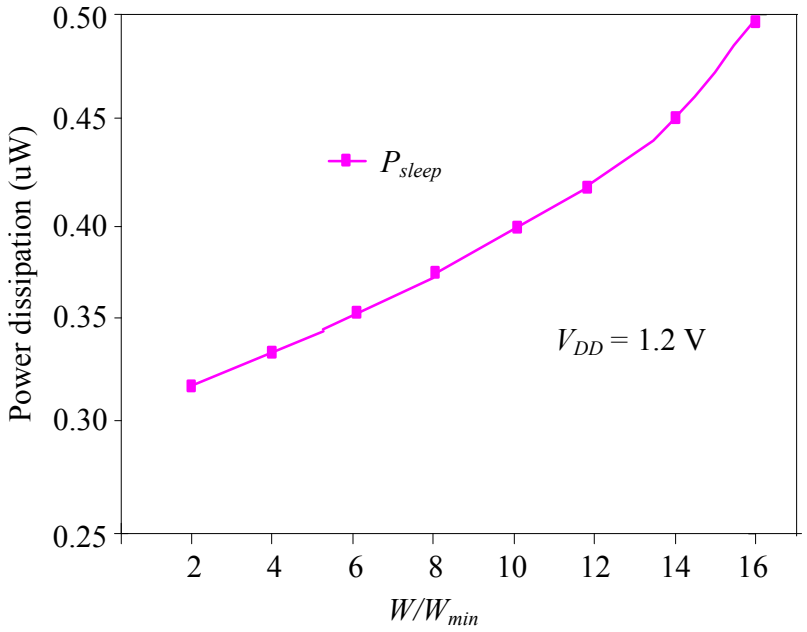


Fig. (10). Power dissipation of power-gating SRMCML buffer/inverter in sleep mode with different width of power-gating PMOS transistor. Channel length of power-gating transistors is 0.13 μm, and W_{min} is 0.195 μm Equivalent model for calculating energy loss in sleep mode.

taken as 0.13 μm, and the channel width ranges from $2W_{min}$ to $16W_{min}$.

The simulated results show that the leakage power dissipation is almost proportional to the channel width of the power-gating transistors. The energy dissipation of the power-gating circuit in sleep mode increases as the channel width of the power-gating transistors increases. From Fig. (**10**), it can be seen that power dissipation of SRMCML buffer/inverter in the sleep mode is much less than the active mode, because only a little leakage current flows through the power source V_{DD}. The simulation results also show that P_{sleep} is almost independence of the bias current. From Fig. (**8**) and Fig. (**10**), P_{active} is about 65 times of P_{sleep} when the channel width of the power-gating transistors is $2W_{min}$, and the bias current is 16 μA. These conclusions prove the correctness of the theories.

4.3. Energy Dissipation for Switching

In order to turn on and off the power-gating PMOS transistors, the additional energy would be dissipated. For turning on the power-gating switch, the node *Sleepb* is charged from Ground to V_{DD}, and the gate voltage (V_{rfp1}) of the power-gating PMOS transistors is discharged from V_{DD} to V_{rfp}. Therefore, energy dissipation for turning on the power-gating switches can be written as

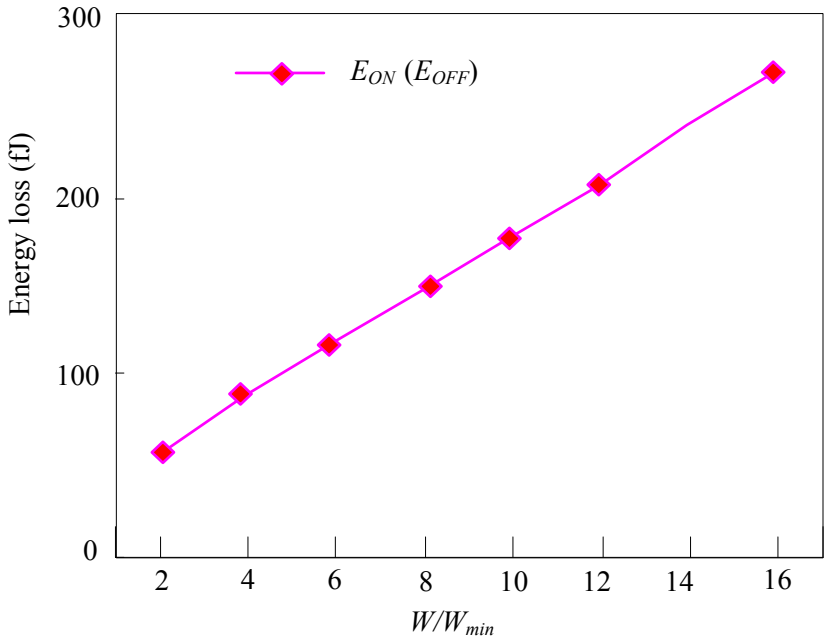


Fig. (11). Energy loss for turning on and off the power-gating switch versus channel width of the power-gating PMOS transistors. Channel length of power-gating transistors is 0.13 µm, and W_{min} is 0.195 µm.

$$E_{ON} = \frac{1}{2} C_{G1} V_{DD}{}^2 + \frac{1}{2} C_{G2} (V_{DD} - V_{rfp})^2 \tag{9}$$

where C_{G1} and C_{G2} are the capacitances of the node *Sleepb* and the gate capacitance of the power-gating PMOS transistors, respectively. Similarly, energy dissipation for turning off the power-gating switch is

$$E_{OFF} = \frac{1}{2} C_{G1} V_{DD}{}^2 + \frac{1}{2} C_{G2} (V_{DD} - V_{rfp})^2 \tag{10}$$

E_{ON} and E_{OFF} are almost the same, which are approximately proportional to the channel width of the power-gating transistors. Fig. (**11**) shows the simulation results of the switching energy dissipations E_{ON} and E_{OFF}. Just as expected, these energy losses are proportional to the channel width of the power-gating transistors.

4.4. Average Power Dissipation

Average power dissipation of power-gating MCML circuits can be calculated as

$$\begin{aligned} P_{AV} &= \frac{E_{active} + E_{sleep} + E_{ON} + E_{OFF}}{T_{active} + T_{sleep}} \\ &= P_{active}\alpha + P_{sleep}(1-\alpha) + \frac{E_{ON} + E_{OFF}}{T_{active} + T_{sleep}} \end{aligned} \tag{11}$$

$$\alpha = T_{active} / (T_{active} + T_{sleep}) \tag{12}$$

where α is power-gating active ratio that is defined as

When the power-gating period (T_{active} + T_{sleep}) is long enough, the energy loss (E_{ON} + E_{OFF}) can be ignored, and thus P_{AV} can be rewritten as

$$P_{AV} \approx P_{active}\alpha + P_{sleep}(1-\alpha) \tag{13}$$

For given source voltage V_{DD}, and bias current I_S, the power dissipation P_{active} keeps constant according to Equation (6). The power dissipations P_{sleep} decrease by reducing the channel width of the power-gating transistors according to Equation (8). Therefore, in order to minimize the power overhead, the channel width of the power-gating transistors should be as small as possible. However, for given ΔV and I_S, the linear resistance of the PMOS transistors has been determined from Equation (3). Therefore, a minimum channel width of the power-gating transistors is limited. In this work, the minimum channel length of the power-gating PMOS transistors was taken with 6λ (2W_{min}).

Fig. (**12**) shows average power dissipation of power-gating SRMCML buffer/inverter with different power-gating activity. In these simulations, the bias current I_S is set as 16 µA. The channel width and length of power-gating transistors are 0.39 µm and 0.13 µm, respectively. From Fig. (**12**), the average power dissipation is almost proportional to power-gating activity because the power dissipation in sleep mode can be ignored for the power-gating activity larger than 0.1.

5. POWER DISSIPATION COMPARISONS

In this section, the power dissipation of the basic SRMCML cells and 1-bit full adder based on power-gating is compared with the basic SRMCML and power-gating static CMOS ones.

The logic function of the 1-bit full adder can be expressed as

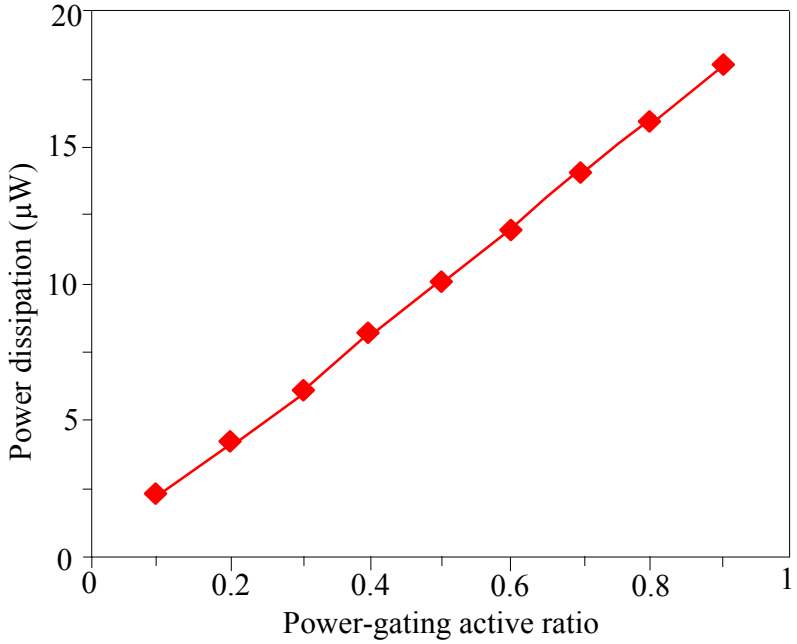


Fig. (12). Power dissipation of power-gating SRMCML buffer/inverter with various power-gating active ratios. The channel width and length of power-gating transistors are 0.39 μm and 0.13 μm, respectively. The biasing current is 16 μA.

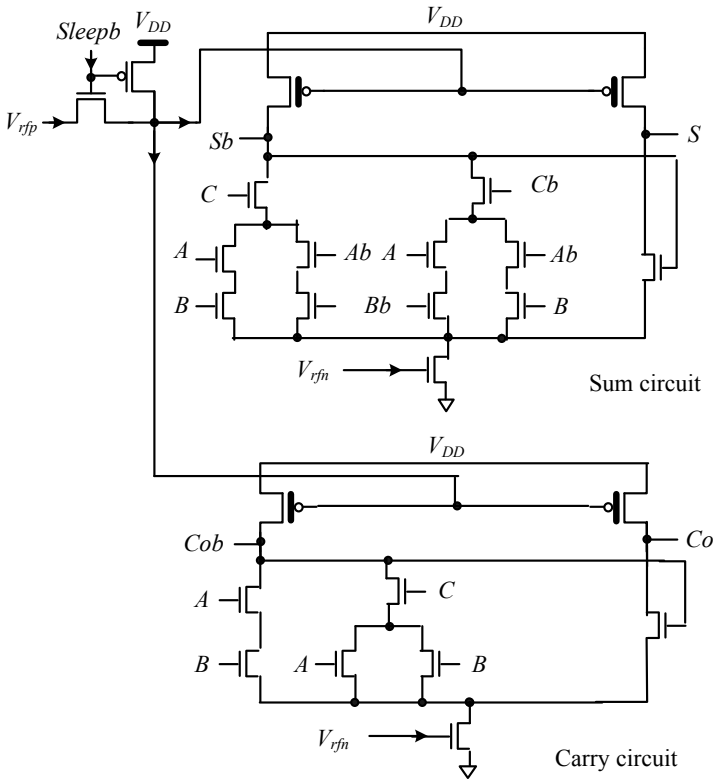


Fig. (13). Power-gating SRMCML 1-bit full adder.

$$S = A \oplus B \oplus C = ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} \quad (14)$$

$$C_O = AB + AC + BC = AB + C(A + B) \quad (15)$$

According to Equation (14) and Equation (15), the 1-bit full adder can be realized by using power-gating SRMCML, as shown in Fig. (**13**). From Fig. (**13**), the complex logic function can be simply realized by using MCML techniques. Therefore, MCML circuits are more suitable to implement the complex circuits.

The basic cells, such as buffer/inverter, OR2/NOR2, OR3/NOR3, AND2/NAND2, AND3/NAND2, multiplexer, XOR2/XNOR2, and 1-bit full adder based on power-gating

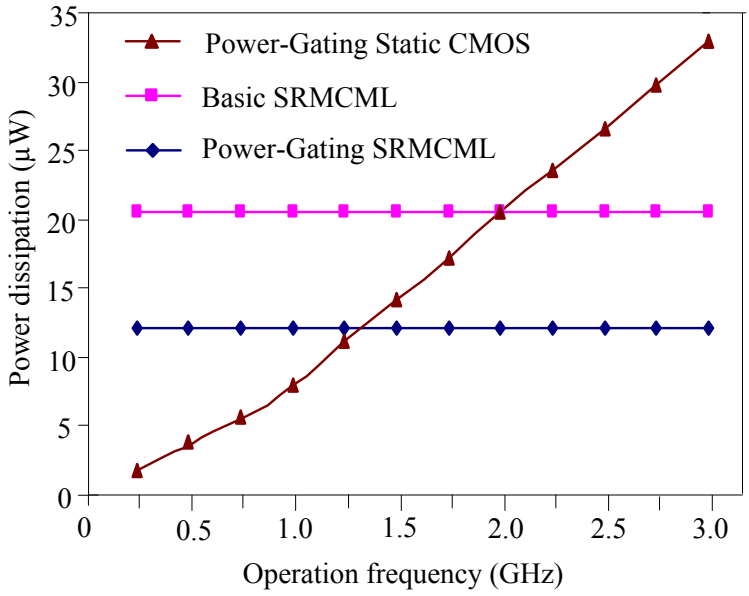


Fig. (14). Power dissipation of buffers/inverters based on power-gating SRMCML, basic SRMCML without power-gating, and power-gating static CMOS. The bias current I_S is 16 μA, and power-gating active ratio α is 0.6.

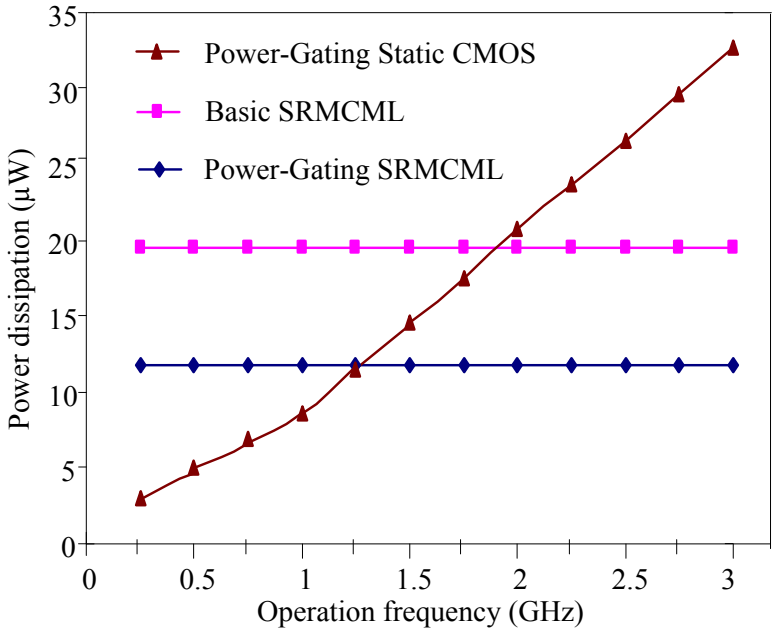


Fig. (15). Power dissipation of two-input OR/NOR gates based on power-gating SRMCML, basic SRMCML without power-gating, and power-gating static CMOS. The bias current I_S is 16 μA, and power-gating active ratio α is 0.6.

SRMCML, basic SRMCML without power-gating, and power-gating static CMOS have been simulated using HSPICE at the 130 nm CMOS process. The simulation results of the power dissipations for buffer/inverter, OR2/NOR2, and 1-bit full adder are shown in the Fig. (**14-16**), respectively.

In these simulations, the operation frequency ranges from 250MHz to 3GHz with a rising step of 250MHz, and the power-gating active ratio α of both SRMCML and conventional CMOS cells is set as 0.6. The device size of the power-gating PMOS transistors was taken with $W / L = 6\lambda / 2\lambda$ (λ=65nm). The bias current I_S of the SRMCML cells is set as 16 μA.

Just as expected, the power consumption of the SRMCML cells is almost independent of operating frequency, while the power consumption of the conventional CMOS cells increases linearly with the operating frequency. The power consumption of the power-gating SRMCML buffer/inverter is lower than the conventional CMOS one in operating frequencies larger than about 1.35 GHz, while the

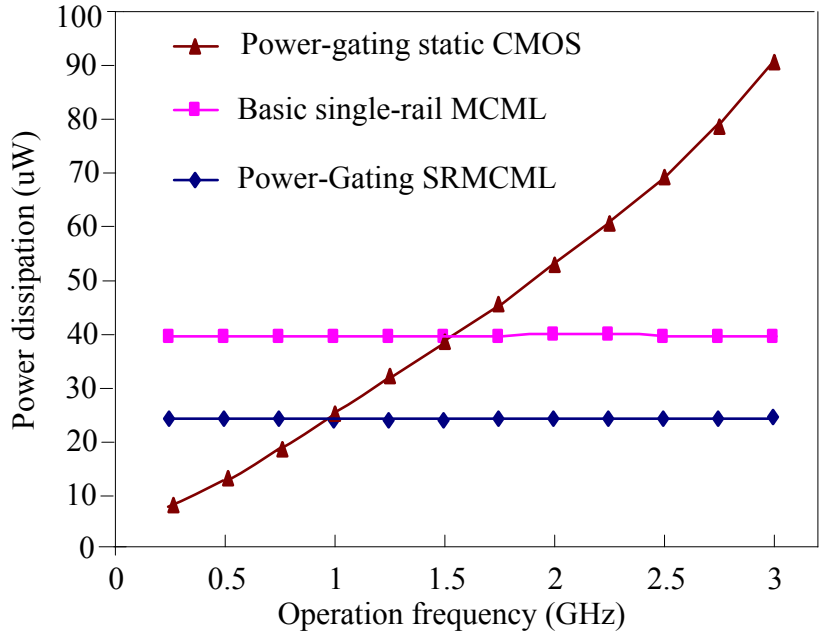


Fig. (16). Power dissipation comparisons among power-gating SRMCML, basic SRMCML and static CMOS 1-bit full adders. The bias current I_S is 16 μA, and the power-gating active ratio α is 0.6.

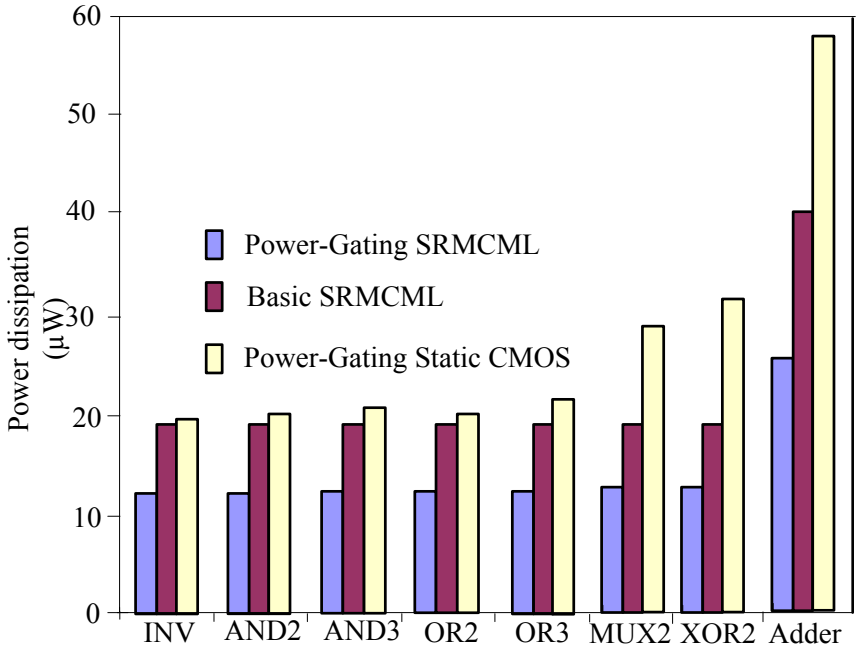


Fig. (17). Power dissipation of basic gates based on power-gating SRMCML, basic SRMCML, and power-gating static CMOS. The bias current I_S is 16 μA. The power-gating active ratio α is 0.6 and operation frequency is 2GHz.

power consumption of the power-gating SRMCML adder is lower than the conventional CMOS one in operating frequencies larger than about 1.0 GHz. This result shows that SRMCML circuits are more suitable to implement the complex circuits in term of power dissipations.

Fig. (**17**) shows the power dissipation comparisons of the basic cells and 1-bit full adder based on power-gating SRMCML, basic SRMCML without power-gating, and power-gating static CMOS at 2 GHz. The power-gating active ratio α of both SRMCML and conventional CMOS cells is set as 0.6. At 2 GHz operating frequency, the power dissipation of the power-gating SRMCML adder is only about 43% of the power dissipation of the conventional CMOS power-gating one.

CONCLUSION

This paper has presented a power-gating scheme for the single-rail MOS Current-Mode Logic (SRMCML), which is used for reducing the power dissipation in the standby mode.

The design methods of the basic power-gating SRMCML circuits are also presented, such as inverter/buffer, AND2/NAND2, AND3/NAND3, OR2/NOR2, OR3/NOR3, XOR2/XNOR2, and 1-bit full adder. The modeling of the sleep transistor in power-gating circuits is constructed and analyzed in detail. The optimization methods of power-gating circuits have be also addressed in tern of energy dissipations. HSPICE simulations show that the power dissipations of the power-gating SRMCML circuits are smaller than corresponding static CMOS alternatives in high-speed applications. In future developments, the power-gating scheme should be applied a large high-speed system.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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