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Low-power Super-threshold FinFET Domino Logic Circuits for High-Speed Applications

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Abstract: Domino logic circuits have faster operating speed than commonly used static logic ones, because they have lower input capacitances and no contention during transition. However, Domino logic circuits have more power dissipation than static logic ones, since their clock tress with high switch activity dissipates large energy. A low-power super-threshold computing scheme is proposed to reduce power dissipations of FinFET Domino logic circuits. The pull-down transistors of all FinFET Domino circuits are configured in parallel, and thus improve operating speed. Unlike near-threshold circuits, super-threshold ones are supplied by much a larger supply voltage than the threshold voltage, but it is lower than the standard supply voltage. Super-threshold FinFET logic circuits can attain low power consumption with favorable performance, because FinFET devices operating on medium strong inversion regions can provide better drive strength than conventional CMOS ones. The basic Domino logic gates are compared with static logic ones in terms of energy consumption, delay, energy delay product (EDP), and maximum operation frequency with different voltages from near-threshold to super-threshold regions. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The results show that the Domino gates can operate faster than static ones. In addition, it is also shown that Domino gates exhibit the best EDP in super-threshold regions (about 700mV). Compared with the standard supply voltage of 1.0 V, the Domino gates supplied by 0.8V can attain energy reductions of more than 38.3% with a small performance penalty of about 14%.

Keywords: Domino logic, FinFET logic circuits, Super-threshold computing, Energy-efficient designs, High-speed designs

INTRODUCTION

In modern IC (Integrated Circuit) designs, high performance with low power and small area is a main objective [1]. The rapid development of CMOS manufacturing processes has greatly increased performance and integration density, and meanwhile reduces the threshold voltage, channel length, and oxide thickness of transistors, resulting in both large dynamic and leakage power dissipations [2]. With the increasing demand for battery-operated electronic products that require ultra-low energy dissipations, high performance with energy-efficient designs have become more and more important [3]. In recent decades of years, IC designers and researcher have been working on faster operation speed with lower power dissipations and smaller chip area [4-6].

Lowering the supply voltage is an effective method to reduce power consumption, since the dynamic and leakage dissipations decrease quadratically and linearly as supply voltage scales down, respectively [7-11]. Sub-threshold or near-threshold circuits can achieve low energy consumption, since their supply voltage is below or slightly above the threshold voltage of the transistors [10]. However, their performance is much lower than these circuits operation on normal source voltages due to the exponential relationship between delay and supply voltage [8].

With the further scaling of CMOS device, the increasing leakage in CMOS circuits caused by short-channel effects and gate-dielectric leakage current has become a main barrier against further scaling [3]. FinFET (Fin-type Feld-Effect Transistors) device with a three-dimensional structure shows low-power characteristic and excellent performance [12]. The recently reported results have been proven that FinFET is a promising alternative for CMOS device to realize continued scaling [13-15].

Domino logic circuits have faster operating speed than commonly used static logic ones, because they have lower input capacitances and no contention during transition [1, 14]. However, Domino logic circuits have more power dissipation than static ones, since their clock tress with high switch activity dissipates large energy. In this work, a low-power super-threshold computing scheme is proposed to reduce power dissipations of FinFET Domino logic circuits. The pull-down transistors of all FinFET Domino circuits are configured in parallel, and thus improve operating speed. Unlike near-threshold circuits, super-threshold ones are supplied by much larger supply voltages than the threshold voltage, but it is lower than the standard supply voltage. Super-threshold FinFET Domino circuits can realize fast operation, since FinFET devices operating on medium strong inversion regions provide strong drive currents. Therefore, it can be

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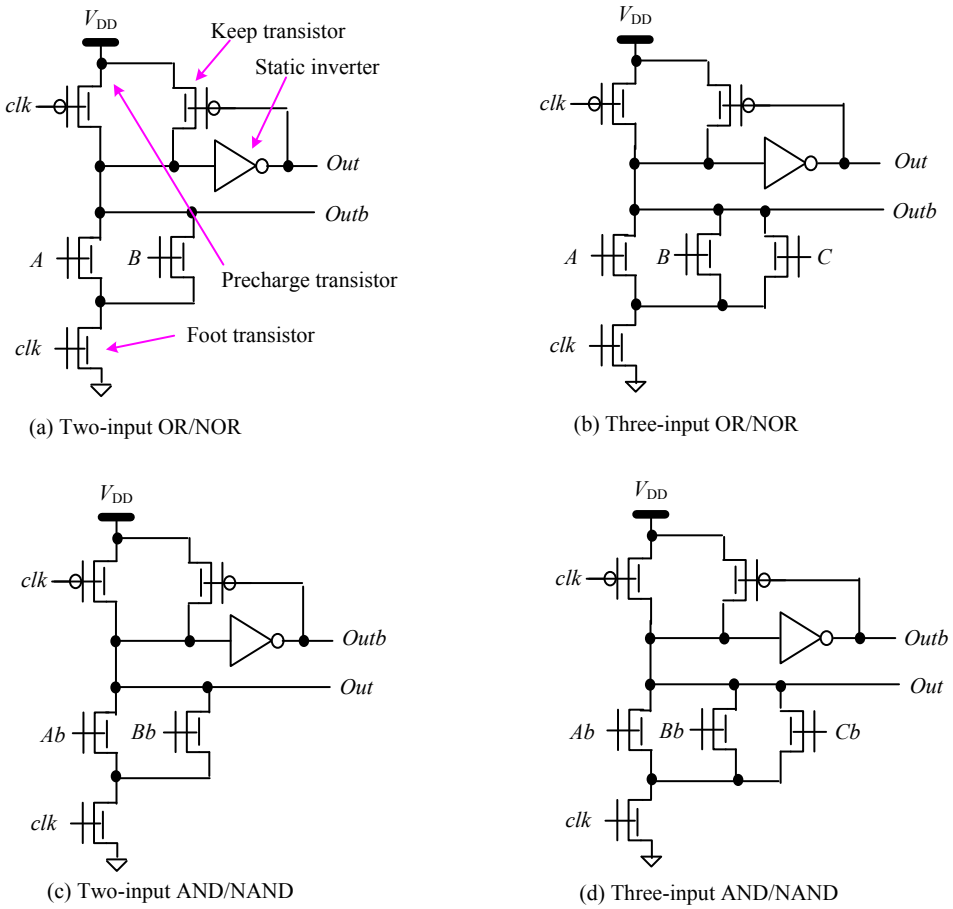

Fig. (1). Two-input and three-input OR/NOR and AND/NAND FinFET gates.

expected that super-threshold computing for FinFET Domino circuits can attain large energy reduction with a small performance penalty compared with the standard source voltage. The basic FinFET Domino logic gates are compared with static FinFET logic ones in terms of energy consumption, delay, energy delay product (EDP), and maximum operation frequency with different voltages. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology [16].

DOMINO FINFET CIRCUITS

In general, dynamic circuits such as Domino logic have faster speed than commonly used static logic ones, because they have lower input capacitances and no contention during transition [1]. However, the series configuration of the logic tree results in performance degeneration at low supply voltages. In the proposed super-threshold scheme, the pull-down transistors of all FinFET Domino circuits are configured in parallel, as shown in Fig. (**1**). The parallel configuration of the N-type FinFET evaluation tree reduces the stack high of transistors, and thus improve operating speed.

The operation of FinFET Domino circuits is divided into two modes. During pre-charge phase, the clock *clk* is 0, so the clocked p-type transistor (Precharge transistor) is ON, and thus initializes the output high. During evaluation phase, the clock is 1 and the clocked p-type transistor turns OFF. The output may remain high or be discharged to low level through the pull-down tree. In Fig. (**1**), a static inverter is added to solve the monotonicity problem of the dynamic circuits. Moreover, in order to reduce leakage and left floating, and increase noise margins, a weak keep p-type transistor is added.

PERFORMANCE COMPARISONS

The energy consumption (E_{total}) of an Domino gate per cycle are expressed as

$$E_{\text{total}} = C_{\text{clk}} V_{\text{DD}}{}^2 + aC_{\text{L}} V_{\text{DD}}{}^2 + V_{\text{DD}} I_{\text{leakage}} T \quad (1)$$

where C_{clk} is gate capacitances of the precharge and foot transistors, a is activity ratio of the output signal, C_L is total node capacitance of the gate, V_{DD} is source voltage, $I_{leakage}$ is average leakage current from supply to the ground, and T is operating cycle. From (1), as supply voltage scales down, the dynamitic and leakage dissipations are reduced quadratically and linearly, respectively.

Assuming that P-type and N-type transistors have symmetrical performance, the delay of a gate can be expressed as

$$t_{\text{d}} = \frac{KC_{\text{L}} V_{DD}}{\left(V_{DD} - V_{\text{th}}\right)^{\alpha}} \quad (2)$$

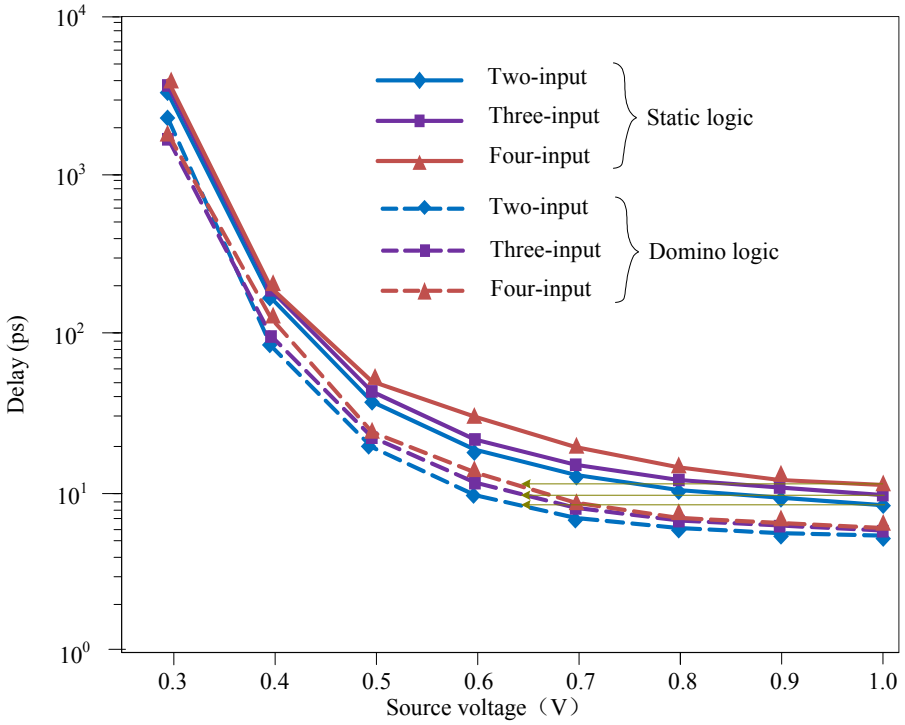

Fig. (2). Propagation delay of 32nm NAND/AND gates based on static and Domino FinFET logic, where the operation frequency is chosen by the minimum value of maximum operation frequencies of the static and Domino logic gates.

where K is fitting parameter, and a is velocity saturation parameter. Energy Delay Product (EDP) is a good compromise between energy dissipation and delay, which is given as

$$EDP = E_{total} \times t_d = \frac{\left(C_L V_{DD}{}^2 + V_{DD} I_{leakage} T\right) K C_L V_{DD}}{\left(V_{DD} - V_{th}\right)^{\alpha}} \quad (3)$$

The gates based on static and Domino logic are simulated with HSPICE at a PTM 32nm FinFET technology. The channel length of all the transistors is taken as L = 32 nm except for the keep transistor, whose channel length is taken as 64 nm. For Domino gates, the fin number of P-type and N-type transistors is taken as 2 except for the keep transistor and static inverter. The fin number of the keep transistor is 1. For the static inverter in the Domino gates, the fin number of P-type and N-type transistors is 2 and 1, respectively. For static NAND gates, the fin number of P-type and N-type transistors is optimized to the same drive strong as Domino gates.

The propagation delay of NAND/AND gates based on static and Domino FinFET logic are compared in Fig. (**2**). The propagation delay of a Domino gate is measured according to the simulation results, which is defined as

$$t_{delay} = \frac{t_{pLH} + t_{pHL}}{2} \quad (4)$$

where t_{pLH} and t_{pHL} are output transition time from low to high level and from high to low level, respectively. The Domino FinFET NAND/AND performs faster than the static ones in all source voltages because of lower input capacitances. At 0.8V source voltage, the two-input, three-input, and four-input Domino gates obtain delay reductions of 41.7%, 46.5%, and 52.1%, compared with static ones, respectively. The more delay reduction can be obtained as the fan-in is increased.

The energy dissipations of NAND/AND gates based on static and Domino FinFET logic are compared in Fig. (**3**). The energy dissipations depend highly on frequencies. In order to assure the comparison fairness, the operating frequency is chosen by the minimum value of the maximum operation frequencies of the two logic styles.

From Fig. (**3**), the Domino logic gates have more power dissipation than static ones, since their clock tress with high switch activity dissipates large energy. From Fig. (**2**) and Fig. (**3**), the Domino gates supplied by 0.8V can attain energy reductions of more than 38.3% with a small performance penalty of about 14%, compared with the standard supply voltage of 1.0 V. Therefore, super-threshold computing for FinFET Domino circuits can attain large energy reduction with a small performance penalty compared with the standard source voltage, since FinFET devices operating on medium strong inversion regions provide strong drive currents.

EDP is compared in Fig. (**4**). The input gate capacitance of the gates is mainly determined by the count of the transistors and their widths. The Domino gates have less stack height than static ones, and thus have less input gate capacitance. As the fan-in is increased, Domino gates use less transistor count, because the evaluation tree of Domino gates uses only N-type transistors. Therefore, the Domino gates obtain less delay because of lower input capacitances and no

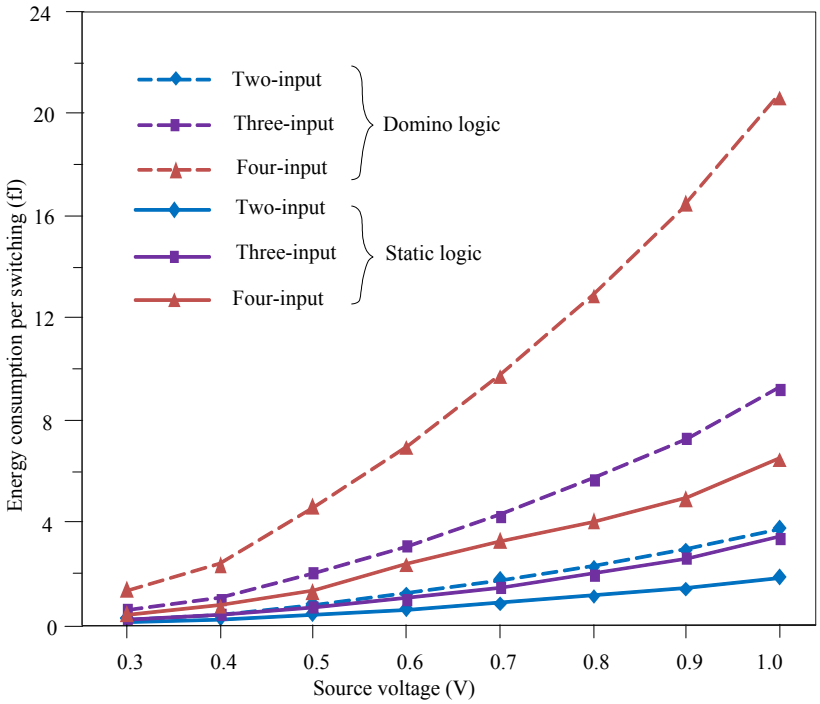

Fig. (3). Energy consumption per switching of 32nm NAND/AND gates based on static and Domino FinFET logic, where the operation frequency is chosen by the minimum value of maximum operation frequencies of the static and Domino logic gates.

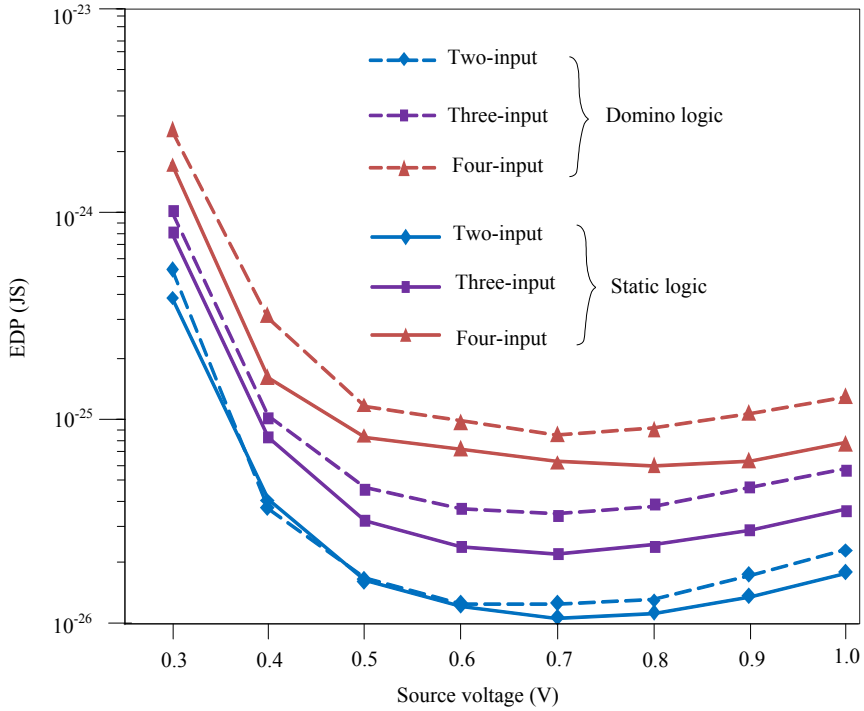

Fig. (4). EDP of 32nm NAND/AND gates based on static and Domino FinFET logic.

contention during transition. However, Domino gates have larger energy dissipations than the static ones, since large energy losses in the clock trees, resulting in larger EDP than the static ones.

Both Domino and static gates achieves the minimum EDP at about 0.7V supply voltage. The two-input, three-input, and four-input Domino gates operating in optimum supply voltages provide an EDP reductions of 44.7%, 39.2%, and 34.5% as compared to nominal supply voltage (1.0V), respectively. At 0.8V source voltage, the two-input, three-input, and four-input Domino FinFET gates obtain energy savings of 39.3%, 38.2% and 37.5%, and EDP reductions of

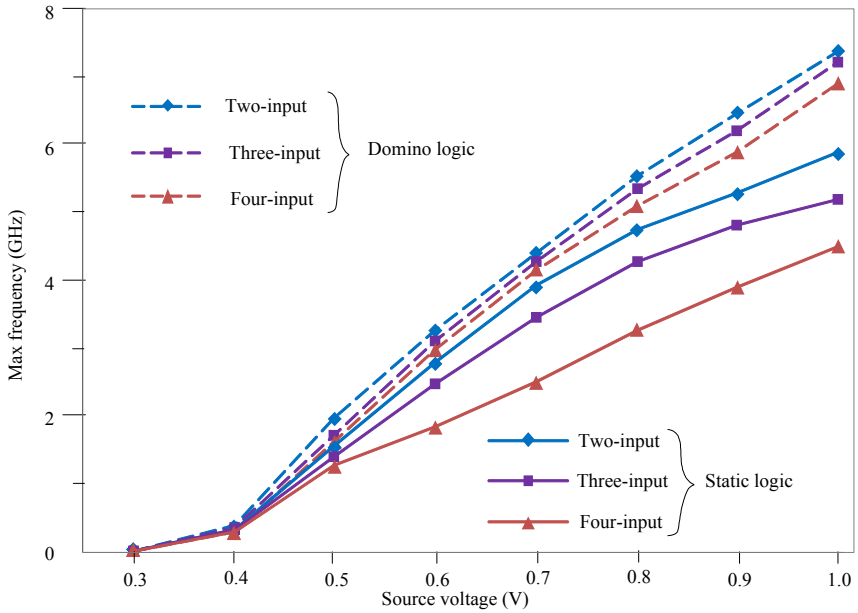

Fig. (5). Maximum operation frequency of 32nm NAND/AND gates based on static and Domino FinFET logic.

42.5%, 34.0% and 30.4%, compared with 1.0V supply voltage, respectively.

The maximum operation frequency are measured according to the simulation results, as shown Fig. (**5**), which is defined as

$$f_{\max} = \frac{1}{T} = \frac{1}{10 \times \left(t_r + t_f\right)} \tag{5}$$

where t_r and t_f are rise and fall times of the gates, respectively.

At 0.8V source voltage, the maximum operation frequency of the two-input, three-input, and four-input Domino gates is as 1.17, 1.25, and 1.56 times as large as the static ones. Compared with 1.0V supply voltage, the Domino gates operating at 0.8V source voltage have only a penalty of about 14% in term of maximum operation frequency. Therefore, Domino circuits operating on super-threshold regions can attain considerable energy saving with a small performance penalty.

CONCLUSION

The rapid development of CMOS manufacturing processes has greatly increased performance and integration density, resulting in both large dynamic and leakage power dissipations. With the increasing demand for battery-operated electronic products, high performance with energy-efficient designs has become more and more important. Domino logic circuits have faster operating speed than commonly used static logic ones. However, Domino logic circuits have more power dissipation than static ones. Lowering the source voltage is an effective method to reduce power consumption, since the dynamic and leakage dissipations decrease quadratically and linearly as supply voltage scales down, respectively. However, lowering the supply voltage to sub-threshold and near-threshold regions would result in a large performance penalty.

In this work, a low-power super-threshold computing scheme have been proposed to reduce power dissipations of FinFET Domino logic circuits. The pull-down transistors of all FinFET Domino circuits are configured in parallel, and thus improve operating speed. Unlike near-threshold circuits, the proposed super-threshold ones are supplied by a much larger supply voltage than the threshold voltage, but it is lower than the standard supply voltage. therefore, the proposed super-threshold FinFET logic circuits can attain low power consumption with favorable performance, because FinFET devices operating on medium strong inversion regions can provide better drive strength than conventional CMOS ones. The basic Domino logic gates have been compared with static logic ones in terms of energy consumption, delay, energy delay product (EDP), and maximum operation frequency with different voltages from near-threshold to super-threshold regions. The results show that the Domino gates can operate faster than static ones. In addition, it is also shown that Domino gates exhibit the best EDP in super-threshold regions (about 700mV). Compared with the standard supply voltage of 1.0 V, the Domino gates supplied by 0.8V can attain energy reductions of more than 38.3% with a small performance penalty of about 14%.

CONFLICT OF INTEREST

The author confirms that this article content has no conflict of interest.

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REFERENCES

[1] N. Weste, and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison-Wesley, Boston, 2010.

[2] L.A Barroso, "The price of performance", *ACM Queue*, vol. 3, no. 1, pp. 48-53, 2005.

[3] N.S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flauyner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan, "Leakage current: moore's law meets static power", *IEEE Computer Magazine*, vol. 36, no. 12, pp. 68-76, 2003.

[4] S. Borkar, A.A. Chien, "The future of microprocessors", *Communications of the ACM*, vol. 54, no. 5, pp. 67-77, 2011.

[5] F. Fallah and M. Pedram, "Standby and active leakage current control and minimization in CMOS VLSI circuits", *IEICE Transactions on Electronics*, vol. E88-C, no. 4, pp. 509-519, 2005.

[6] W. Zhang, L. Su, Y. Zhang, L. Li, and J. Hu, "Low-leakage flip-flops based on dual-threshold and multiple leakage reduction techniques", *Journal of Circuits, Systems and Computers*, vol. 20, no. 1, pp. 147-162, 2011.

[7] R. Vaddi, S. Dasgupta, and R.P. Agarwal, "Device and circuit co-design robustness studies in the subthreshold logic for ultralow-power applications for 32 nm CMOS", *IEEE Transactions on Electronic Devices*, vol. 57, no. 3, pp. 654-664, 2010.

[8] K. Gupta, A. Raychowdhury, and K. Roy, "Digital computation in subthreshold region for ultralow-power operation: A device–circuit–architecture codesign perspective", *Proceedings of the IEEE*, vol. 98, no. 2, pp. 160-190, 2010.

[9] M. Srivastav, M.B. Henry, and L. Nazhandali, "Design of energy-efficient, adaptable throughput systems at near/sub-threshold voltage", *ACM Transactions on Design Automation of Electronic Systems*, vol. 18, no. 1, pp. 1-23, 2013.

[10] R.G. Dreslinski, M. Wieckowski, D. Blaauw, and D. Sylvester, "Near-threshold computing: Reclaiming moore's law through energy efficient integrated circuits", *Proceedings of the IEEE*, vol. 98, no. 2, pp. 253-266, 2010.

[11] J. Hu, and X. Yu, "Low voltage and low power pulse flip-flops in nanometer cmos processes", *Current Nanoscience*, vol. 8, no. 1, pp. 102-107, 2012.

[12] D. Hisamoto, W.C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kua, E. Anderson, T.J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm", *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320-2325, 2000.

[13] M. Rostami, and K. Mohanram, "Dual-Vth independent-gate FinFETs for low power logic circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 30, no. 3, pp. 337-349, 2011.

[14] A.T. Sherif, and K. Volkan, "FinFET domino logic with independent gate keepers", *Microelectronics Journal*, vol. 40, no. 11, pp. 1531-1540, 2009.

[15] W. Zhang, J.G. Fossum, L. Mathew, and Y. Du, "Physical insights regarding design and performance of independent-gate FinFETs", *IEEE Transactions on Election Devices*, vol. 52, no. 10, pp. 2198-2206, 2005.

[16] N. Paydavosi, S. Venugopalan, Y.S. Chauhan, J.P. Duarte, S. Jandhyala, A.M. Niknejad, and C. Hu, "BSIM—SPICE models enable FinFET and UTB IC designs", *IEEE Acess*, vol. 1, pp. 201-215, 2013.

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