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Design and Implementation of Data Processing Platform Based on Virtual Instrument

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Abstract: In order to the meet the requirements for the timeliness and the large data volume of the data transmission of the towed linear array sonar system, a kind of data recording system based on PCI is designed. In the aspect of hardware, the system employs the scheme combining PCI9054 efficient DMA transmission technology and the external-expansion large-capacity FIFO to realize the high-speed and continuous sonar data transmission; in the aspect of software, the system combines the memory mapping file based on dual-layer ping-pong structure and multithreading technology to realize the real-time storage, processing and displaying of the data. The results of the simulation and field experiments show that this recording system can stably and reliably realize such functions as real-time storage and waveform display-back of the sonar data, thus able to meet the data recording requirement of large sonar system.

Keywords: Towed linear array, Sonar, Data recording System, Dual-layer ping-pong structure memory mapping, Multithreading technology.

1. INTRODUCTION

The towed linear array sonar plays an important role in the aspects of ocean exploration, oceanographic engineering, military naval warfare, marine science research, etc. [1, 2]. Therein, the data recording system acts as a bridge for the information transmission between underwater towed linear sonar subsystem and computer system. Due to large sonar data volume and high transmission timeliness, in order to reliably transmit underwater towed linear array sonar data to computer system for real-time storage, it is necessary to adopt the high-speed computer bus technology to realize the design of sonar data recording system [3, 4]. According to the hierarchical position of the bus in the system mechanism, the computer bus is currently mainly divided into on-chip bus, internal bus and external bus [5], wherein the internal bus (also called system bus mainly including STD, ISA, PCI buses, etc.) and the external bus (mainly including RS-232, USB bus, IEEE-488 bus, etc.) can be used for peripheral equipment communication. Additionally, the external bus is usually used for the parts not having strict requirement for the transmission speed, e.g. RS-232 serial interface or USB interface; however, PCI bus [6] is frequently used for computer application. According to the above comprehensive analysis, due to the features of high transmission timeliness and large data volume of sonar signal, PCI bus is used in the article as the computer interface in order to design a kind of towed linear array sonar data recording system based on PCI bus. This system employs PCI bridged chip 9054 to realize DMA transmission and meanwhile combines the dual-layer ping-pong structure memory mapping file and multithreading parallel processing technology to realize the real-time acquisition, storage, processing and displaying of towed linear array sonar signal.

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2. GENERAL SYSTEM SCHEME AND SYSTEM INDEX

2.1. System Structure and Scheme

The towed linear sonar system structure is as shown in Fig. (**1**). According to the position, the whole sonar system can be divided into two parts, namely on-board equipment and subsea equipment, wherein the core of the subsea equipment is sonar detection towline mainly composed of sensing element, digital packet, header packet, command/synchronization downlink channel and data uplink channel. Specifically, the digital packet is composed of acquisition module and transmission module, wherein each acquisition module includes 16 channels and each channel can carry out 24bitAD conversion and the signal sampling rate is 4 KHz.

2.2. Main System Indexes

According to the design requirements of a certain military project, the towed linear array sonar data recording system shall have the capability of receiving and processing the data from 512 sensing elements in a real-time manner. More

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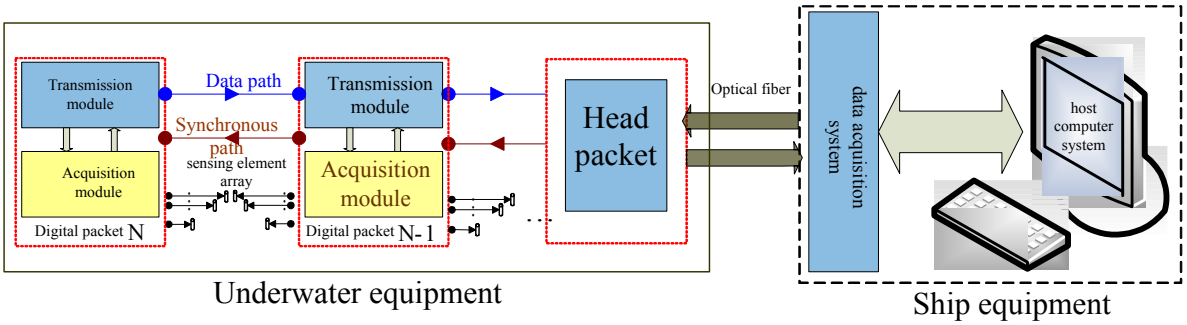

Fig. (1). Towed Linear Sonar System Structure.

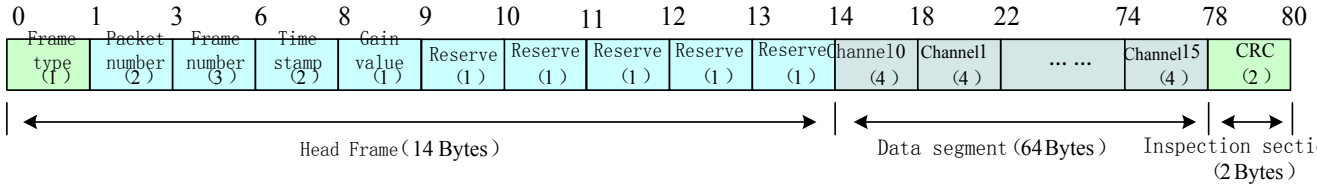

Fig. (2). Data Frame Format.

specifically, according to the design scheme in section 1.1 and the project requirements, the sonar detection towline shall be composed of at least 32 data packets and each data packet shall acquire the sonar data of 16 channels; according to the index requirement, ADC of each channel employs 24bit AD converter and the sampling rate is 4 KHz. Therefore, the total net data rate V_t of the sonar detection system is:

$$V_t = 32 \times 16 \times 24 \times 4000 = 49.152\,M(bps) \quad (1)$$

According to the transmission protocol designed and defined in the project, each data packet will compile the data acquired by the acquisition module from 16 sensing elements at each time into an integral data frame and transmit to the superior level. Therein, the data frame includes 80 bytes in total and each byte is 8 bits, with the format as shown in Fig. (**2**).

The data frame includes 14-byte frame header, 64-byte data segment and 2-byte CRC verification segment, wherein the frame header is used to identify each digital packet, data frame type, digital packet No., frame No., time stamp, gain value, system expansion space reservation and other information; the data segment is used to store the data acquired from 16 sensing elements, and each acquisition channel acquires 4-byte data at each time, namely 32 bits.

In order to strengthen the data transmission reliability in line, 8B10B encoded sonar data are transmitted. Therefore, according to the above analysis, the transmission rate V_m of the whole sonar detection system is:

$$V_m = 32 \times (16 \times 4 + 14 + 2) \times 4000 \times 10 = 102.4\,M(bps) \quad (2)$$

According to formula (2), in order to meet system requirements, the towed linear array sonar data recording system must have very strong capacity of converting, transmitting and processing data in a real-time manner.

3. TOWED LINEAR ARRAY DATA PROCESSING SYSTEM

3.1. Data-Caching Scheme

In order to ensure the reliable and stable transmission of high-speed data, the design scheme for the data-caching module is crucially important. Dual SDRAM ping-pong structure is usually used in such data-caching scheme. However, on the one hand, SDRAM is based on addressing mode access, has many address wires and needs to occupy a lot of IO interface resources; on the other hand, it has the features of dynamic refresh and complicated control time sequence. Therefore, such recoding system adopts external-expansion FIFO chip for the design of data-caching module; with simple control logic and high reliability, FIFO does not need complicated addressing operation.

PCI9054 employs DMA mode to read sonar data from FIFO and upload to computer through the interrupted trigger. The data are continuously uploaded by the underwater towed system and the computer interruption response time is long and uncertain, so FIFO is used to cache data to compensate the interrupted response time so as to realize the integrity and the real-time storage of the data. More specifically, in order to continuously upload the data from the towed system to the computer for storage, it is necessary to meet the following conditions: the time T_1 for writing sonar data into FIFO must be longer than the time T_2 for the computer to read data from FIFO.

According to relevant data and tests, the computer interruption response time is 100~125us. Under ideal condition, f_R, namely the clock frequency for PCI9054 to read data, is

Table 1. FIFO Depth Selection Basis.

No.	f_W /(MHz)	L
1	3	426 *2=852(1k)
2	5	781*2=1562(2k)
3	10	2083*2=4166(5k)
4	15	4687.5*2=9375(10k)
5	20	12500*2=25000(25k)
6	23	35937.5*2=71875(71k)

Table 2. Maximum Transmission Rate Test Result.

No.	f_W /(MHz)	V_W /(MB/s)	δ
1	5	20	0
2	15	60	0
3	20	80	0
4	24	96	0
5	25	100	5%

maximally as 33MHz; according to the actual measurement, in efficient transmission Continuous Burst mode, the average DMA speed is 100MB/s [7-9], namely $f_R = 25MHz$. The clock frequency for writing sonar data into FIFO is f_W, FIFO byte width is 32 bits and the depth is L, then:

$$T_1 = L \bullet f_W \tag{3}$$

$$T_2 = L \bullet f_R + 125us \tag{4}$$

$$T_1 \geq T_2 \tag{5}$$

The FIFO depth selection basis can be deduced from formulae (3), (4) and (5), as shown in Table **1**.

According to formula (2), the speed for writing sonar data into FIFO is 102.4Mbps, and PCI bus length is 32 bits, so the clock frequency for writing data into FIFO is 102.4/32=3.2MHz. If $f_W = 5MHz$, then L =2k is enough.

According to above analysis, it is only necessary to select the FIFO with the storage capacity over 2k to meet the data-caching requirement of the system; however, in order to not only reserve certain hardware for practical design, but also facilitate the expansion of the sonar towline in future, a kind of synchronous FIFO, IDT72V36110 is selected for the system, wherein the depth thereof is 128k and the width thereof is 36bit; if 32-bit word width is used for data storage, then the total caching capacity is 4.096Mbit [10-12].

3.2. Hardware Structure of Towed Linear Array Sonar Data Recording System

The hardware structure of the data recording system is as shown in Fig. (**3**). The system is composed of photoelectric receiving and dispatching module, serial-parallel/parallel-serial conversion module, logic control module, FIFO caching module and PCI9054 interface module. Therein, on the one hand, the photoelectric receiving and dispatching module converts the electrical command signal issued by the computer into optical signal and dispatches it to the towed sonar system; on the other hand, the photoelectric receiving and dispatching module converts the optical signal uploaded by the towed sonar system into electrical signal and dispatches it to the recording system. The serial-parallel/ parallel-serial conversion module is mainly composed of MAX9206 and MAX9205 and is used to realize serial-parallel/parallel-serial data conversion. The logic control module is mainly composed of FPGA; on the one hand, this module processes and dispatches the command information issued by the computer; on the other hand, this module controls the caching and uploading of the sonar data [13, 14]. FIFO caching module is used to cache sonar data. PCI9054 interface module takes out sonar data from FIFO through DMA mode, timely and speedily uploads the sonar data to computer memory.

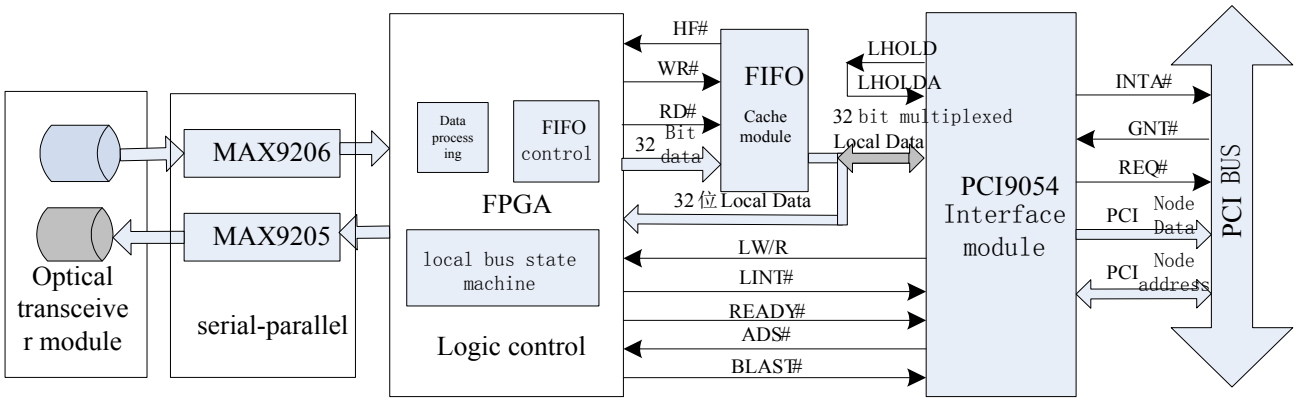

Fig. (3). Hardware Structure of Data Recording System.

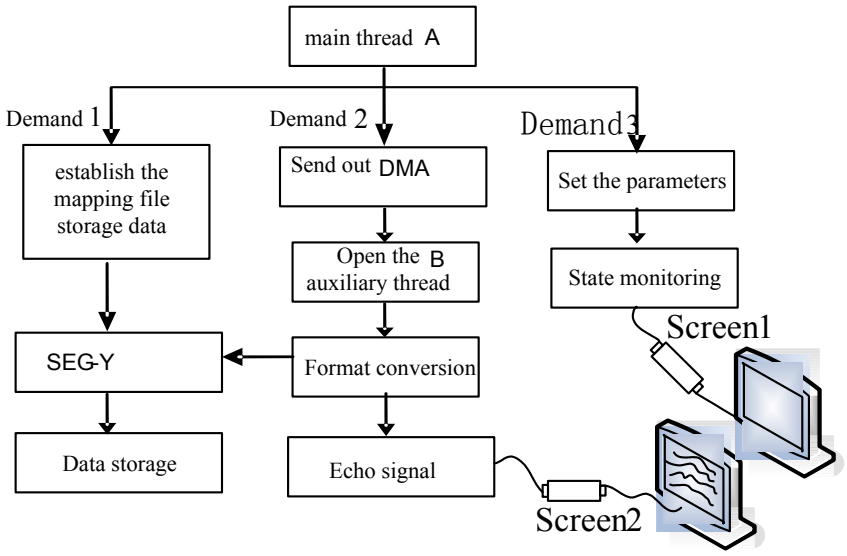

Fig. (4). Software Design Block Diagram.

4. UPPER COMPUTER SOFTWARE DESIGN FOR TOWED LINEAR ARRAY SONAR DATA RECORDING SYSTEM

The upper computer software is the control center of the sonar data recording system and is mainly responsible for dynamically configuring and dispatching subsea equipment (e.g. sensing element, acquisition board, transmission board, redundancy backup board) and controlling the operating state of the whole sonar detection system as well as timely recording, processing and displaying the sonar data, etc. Object-oriented visual integrated programming system Visual C++ is adopted for the design as the development environment in order to realize format conversion, storage and graphic monitoring of large-volume data [15-17]. The main control software design framework is as shown in Fig. (**4**). The main control software is mainly used to complete the three software requirements indicated in Fig. (**4**), and the three requirements are realized through the multithreading concurrent execution mode, wherein requirement 1 aims at timely storing the sonar data through dual-layer ping-pong structure memory mapping file mode while requirements 2 & 3 aim at receiving and displaying the sonar data as well as controlling the operating state of the system.

4.1. Multithreading Technology

After the software is started, the main control software maintains the normal operation thereof through main thread A and displays the operating state of the sonar detection system through Screen 1. After the data acquisition initialization, the auxiliary thread B for data acquisition is started to convert the data frame transmitted by the acquisition subsystem into intermediate format data; afterwards, on the one hand, the intermediate format file is converted into standard sonar detection SEG-Y format file for storage; on the other hand, the waveform of the intermediate format data is displayed on Screen 2 to meet the requirement for friendly man-machine interaction.

The data volume of the system will be increased along with the increment of the sensing elements, and the processing task involving such large data volume will bring adverse effect to the real-time processing and displaying of the data waveform, so the system adopts multithreading concurrent execution technology in the process of displaying back the data waveform. Firstly, all elements are divided into multiple primitive data groups according to the position relationship of the elements and the data of each primitive data group is provided with one data buffer of which size shall be

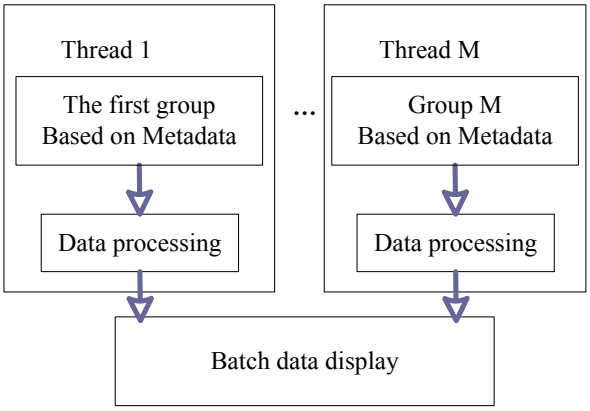

Fig. (5). Multithreading Data Processing Method.

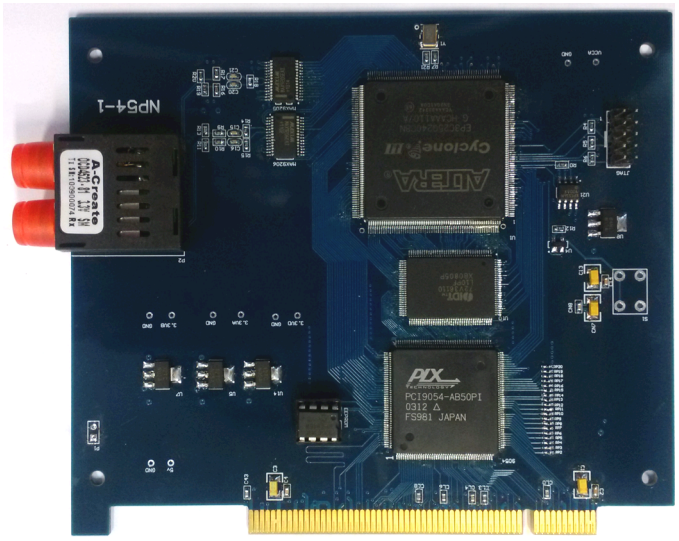

Fig. (6). Data Recording System Hardware.

able to display and output the sonar data on one screen; then, one secondary thread is defined for each primitive data group. After the operator inputs the primitive data group to be displayed through the human-computer interaction interface, the corresponding secondary thread is initiated to process the data; after batch data processing, the main thread is initiated to display the processing result. The multithreading data processing method is as shown in Fig. (**5**).

4.2. Real-Time Storage of Sonar Data Through Dual-layer Ping-Pong Structure Memory Mapping File Mode

The data acquisition subsystem continuously uploads data streams, but it takes long time to establish storage file, and if the new file is established after one storage file is maximally utilized, the data uploaded by PCI will be lost during the period of establishing the new file. In order to solve the above problem, the system employs dual-layer ping-pong structure memory mapping file mode to realize the real-time storage of the sonar data.

When using memory mapping file to process the files stored on the disk, there is no need to execute I/O operations for the relevant files, because the memory mapping file plays an important role in processing large data volume files. Therein, the memory mapping refers to the mapping from one file to the process address space [10]. One address space area is firstly reserved through the memory mapping file and meanwhile such physical storage is submitted to this area, wherein the physical storage mapped by the memory file is sourced from the file already stored on the disk. Before file operation, the file must be firstly mapped.

5. EXPERIMENTS

The data recording system hardware is as shown in Fig. (**6**).

On the one hand, Experiment 1 is designed to verify whether the data recording system can meet the design requirements of the towed linear array sonar system (512 sensing elements); on the other hand, as described in the previous

Fig. (7). Error Rate Test Result.

section, we select and use the FIFO caching module with the calculation capacity greater than the theoretically calculated volume in order to facilitate the further expansion of the sonar towline in future; the recording system based on FIFO caching module shall have stronger data receiving and transmitting capability, so Experiment 2 is designed to further test the maximum rate for the recording subsystem to reliably and stably transmit data.

Experiment I: error rate test

Basic thought for error rate test: simulate the generation of the real sonar data frame in FPGA and compare the received data and the transmitted data in the computer to judge data error rate δ generated during the transmission process, namely:

$$\delta=\frac{The\ number\ of\ error\ bits}{The\ total\ number\ of\ bits\ transmitted} \quad (6)$$

The specific realization process is as follows: (i) Firstly simulate the continuous generation of sonar data frames in FPGA as shown in Fig. (**4**) according to data transmission protocol; set the transmission rate of writing data into FIFO as 102.4Mbps (according to formula (2)); adopt 80-byte data frame (as shown in Fig. **2**) mentioned in the transmission protocol as the data frame format, wherein 64-byte data segment carries the sonar data acquired by 16 channels (32 bits for each channel) and the data of each channel is set as 32-bit data gradually accumulated by 1 from 0. (ii) Secondly, adopt the data recording system mentioned in the article to transmit and receive data. More specifically, store the received data, and then design corresponding data comparison method to compare the received data and the transmitted data and meanwhile record the error bits.

Transmit 1GB data for each time at the transmitting end, compare and store the received data in the computer, as shown in Fig. (**7**), and repeat the experiment for 20 times, wherein the error rate of data transmission and receiving is 0. Therefore, the result of the repeated experiments has verified that the recording system can stably and reliably meet the design requirements of the towed linear array sonar system.

Experiment II: maximum transmission rate test

Similar to Experiment I, simulate the generation of real sonar data frames in FPGA and compare the received data and the transmitted data in the computer to test the error rate δ. Notice: it is necessary to gradually increase the click frequency f_W for writing the simulation data into FIFO during the test process in order to increase the data transmission rate V_W, and repeat the experiment for each determined f_W for 20 times. The experiment result is as shown in Fig. (**2**).

Conclusion obtained from the experiment result: the maximum inerrant data transmission rate of the data recording system is 96MB/s.

CONCLUSION

In allusion to the high timeliness and large data volume of the towed linear array sonar data transmission, a kind of towed linear array sonar data recording system based on PCI bus is designed, wherein the maximum continuous data transmission rate available for the data recording system is 96MB/s; and meanwhile the memory mapping file based on dual-layer ping-pong structure is adopted for the real-time storage of the sonar data; and the multithreading concurrent execution technology is adopted for the real-time processing and displaying of the data. The towed linear sonar system has been tested in Qilihai, Tianjin, and the test result shows that the system can stably and reliably run, and timely store the data, as well as display back the waveform within the preset time interval, thus to well meet the design requirement for a certain military project.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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REFERENCES

[1] M. Zhang, Z. Lv, X.. Zhang, G. Chen, and K. Zhang. "Research and Application of the 3D Virtual Community Based on WEBVR and RIA," *Computer and Information Science,* vol. 2, no. 1,pp. 84, 2009.

[2] T. Su, Zhihan. Lv, S. Gao, X. Li, and H.Lv, "3D seabed: 3D modeling and visualization platform for the seabed," In: *Multimedia and Expo Workshops (ICMEW)*, IEEE International Conference on, pp. 1-6, 2014.

[3] X. Li, Z. Lv, B. Zhang, W. Wang, S. Feng, and J. Hu, "WebVRGIS Based City Bigdata 3D Visualization and Analysis." In: *Pacific Visualization Symposium (PacificVis)*, 2015.

[4] S. Li, Y. Geng, J. He, and K. Pahlavan, "Analysis of Three-dimensional Maximum Likelihood Algorithm for Capsule Endoscopy Localization," 5th International Conference on *Biomedical Engineering and Informatics (BMEI)*, Chongqing, China, pp. 721-725, 2012.

[5] T. Alex, B. Laurent, M. Piuzzi, Z. Lu, M. Chavent, M. Baaden, and O. Delalande, "Advances in Human-Protein Interaction-Interactive and Immersive Molecular Simulations," *InTech*, 2012.

[6] Z. Chen, S. M. Arisona, X. Huang, M. Batty, and G. Schmitt, "Detecting the dynamics of urban structure through spatial network analysis," *International Journal of Geographical Information Science,* vol. 28, no. 11, pp. 2178-2199, 2014.

[7] R. Ma, Z. Lv, Y. Han, and G. Chen, "Research and Implementation of Geocoding Searching and Lambert Projection Transformation Based on WebGIS," *Geospatial Information,* vol. 5, pp. 013, 2009.

[8] J. Wang, Z. Lv, X. Zhang, J. Fang, and G. Chen, "3D Graphic Engine Research Based on Flash," *Henan Science,* vol. 4, pp. 015, 2010.

[9] Y. Geng, and K. Pahlavan, "On the Accuracy of RF and Image Processing Based Hybrid Localization for Wireless Capsule Endoscopy," *IEEE Wireless Communications and Networking Conference (WCNC)*, 2015.

[10] J. He, Y. Geng and K. Pahlavan, "Toward Accurate Human Tracking: Modelling Time-of-Arrival for Wireless Wearable Sensors in Multipath Environment," *IEEE Sensor Journal*, vol. 14, no.11, pp. 3996-4006, 2014.

[11] M. Zhang, Z. Lv, X. Zhang, G. Chen, and K. Zhang, "Research and Application of the 3D Virtual Community Based on WEBVR and RIA," *Computer and Information Science,* vol. 2, no. 1, pp.84, 2009.

[12] T. Su, Zhihan. Lv, S. Gao, X. Li, and H. Lv, "3D seabed: 3D modeling and visualization platform for the seabed," In *Multimedia and Expo Workshops (ICMEW)*, 2014 IEEE International Conference on, pp. 1-6, 2014.

[13] D. Jiang, Z. Xu, P. Zhang, and T. Zhu, "A transform domain-based anomaly detection approach to network-wide traffic," *Journal of Network and Computer Applications,* vol. 40, pp. 292-306, 2014.

[14] Y. Geng, J. He, H. Deng and K. Pahlavan, "Modeling the Effect of Human Body on TOA Ranging for Indoor Human Tracking with Wrist Mounted Sensor," 16th International Symposium on *Wireless Personal Multimedia Communications (WPMC)*, Atlantic City, NJ, 2013.

[15] Z. Lv, A. Halawani, S. Feng, H. Li, and S. Ur Réhman, "Multimodal Hand and Foot Gesture Interaction for Handheld Devices," ACM Transactions on Multimedia Computing, *Communications, and Applications* (TOMM) vol. 11, no. 1, pp. 10, 2014.

[16] Z. Lv, T. Yin, Y. Han, Y. Chen, and G. Chen, "WebVR——web virtual reality engine based on P2P network," *Journal of Networks,* vol. 6, no. 7, pp. 990-998, 2011.

[17] Z. Lv, L. Feng, H. Li, and S. Feng, "Hand-free motion interaction on Google Glass," In*: SIGGRAPH Asia Mobile Graphics and Interactive Applications*, pp. 21, ACM, 2014.

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