Send Orders for Reprints to reprints@benthamscience.ae

The Design of Radar Digital Intermediate Frequency Test System

Han Bin*

College of Information Security Engineering, Chengdu University of Information Technology, Chengdu, 610225, China

Abstract: To satisfy the requirement of high performance signal processing technique, it is necessary to use the direct sampling of intermediate frequency signal to obtain quadrature signals. Digital intermediate frequency (DIF) system is widely used in radar and communication system. This paper briefly introduces the principle of test system based on DIF. We design this DIF test system to test the performance of ADC and I/Q. The design has the advantages of convenient use, and reliable performance.

Keywords: Digital intermediate frequency, radar, test system.

1. INTRODUCTION

In many radar, sonar and communication systems, it needs to translate the output signal of receiver into two channel quadrature signals, *i.e.* is I (in-phase) signal and Q (quadrature) signal. Because it carries the phase information of the signal, the two baseband signal is used for coherent integration. So, the receiver which uses quadrature coherent detection technology has a greater dynamic range and higher precision than the receiver which does not use it.

Radar digital Intermediate Frequency (IF) receiver is designed for the modern radar receiver which is developed with more high-tech and high-performance specification. Radar digital IF receiver makes the IF signal digital directly using the high-performance digital acquisition system and advanced digital signal processing technology. Radar digital IF receiver can get a larger linear dynamic range and a perfect I/Q signal quality, and thus it can improve the performance of the radar system [8]. In a digital IF system, we send the radar echo data into the IF to perform high-speed AD sampling, through digital down conversion, through data buffer, which final becomes the I (in-phase) and Q (quadrature) parallel data stream (each is 24 bit) whose rate is 2.4 Mbit/s. The two baseband signal can be used for coherent integration because it carries the phase information of the signal. So, it can get larger linear dynamic range and higher accuracy which the receiver uses in the orthogonal detection technology [3, 4].

It is a very important and valuable work to test the performance of ADC and I/Q of the radar digital IF. By evaluating its performance about ADC and I/Q, We can confirm whether it meets the requirements, also we can find the major factor which influence the system performance, so that the system can be improved further. The test system can help us find and solve the problem of the digital IF quickly. So we design a digital IF test system based on USB interface, which can not only analyze the performance of A/D sampling and I/Q signal, but also it is the powerful tool for entire IF system.

*Address correspondence to this author at the collage of Information Security Engineering, Chengdu University of Information Technology, Chengdu, Sichuan, 610225, P.R. China; Tel: 8613882042733;
E-mail: hanbin@cuit.edu.cn

2. THE PRINCIPLE OF DIGITAL QUADRATURE SAMPLING

Unlike the traditional signal processing, intermediate frequency demodulation uses simulated complex demodulation method. The basic principle is that it uses a phase-locked loop and oscillator which is controlled by voltage to generate two orthogonal frequency carrier signals. The input frequency signal is migrated to the frequency domain and multiplied with analog multiplier and two orthogonal frequency carrier signals [5-7].

3. THE CONSTITUTION OF THE SYSTEM

The test system is made up of two parts: module of ADC test and module of I/Q test. This test system has two independent test cards and software. The whole system is small; installation is convenient; and its testing is very flexible because the system uses the USB interface. The system structure is shown in Fig. (**1**).

The system is composed of three modules: data receiving module, data transmission module, and data analysis module. The data receiving module is responsible for the ADC and I/Q output interface connected data acquisition. Transmission module is used for data transmission from the card to the host, and the software module, for data analysis and processing.

In this Digital IF test system, ADC sampling uses the ultra-high-speed sampling chip- AD6644 (14bits/65MHz). ADC performance directly affects the Index of the Digital IF. In the ADC test, ADC data storage using the chip of IDT Company, the storage chip is high speed FIFO chip: IDT72V2105L10PF, its capacity is 256K× 18bit. Memory Access speed is 10ns. In the test card, It has the FIFO depth

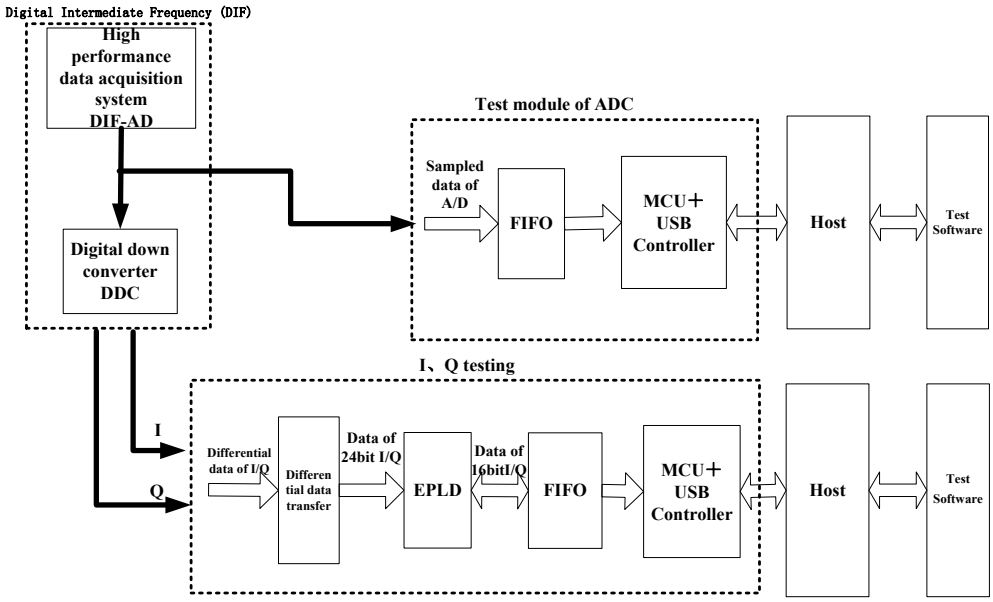

Fig. (1). Digital IF test system block diagram.

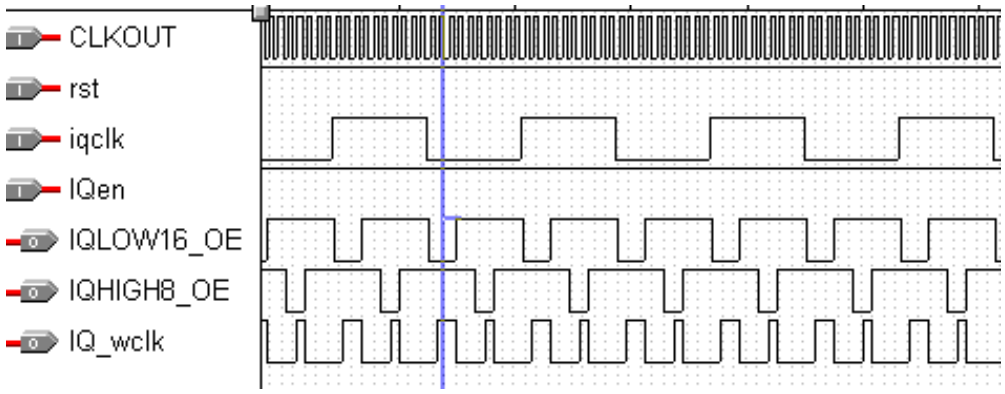

Fig. (2). Time of I/Q test FIFO.

expansion for high capacity data application. FIFO writes clock using intermediate frequency system clock ADCLK.

I/Q test card receives 62 route differential data, and converts the data into 24 bits I/Q data and other control signals by using the AM26LS32 chip. The I signal is rising at the edge of the IQCLK clock signal; the Q signal is falling at the edge of the IQCLK clock signal. This design uses the Altera company EPLD chip which is named EPM7128, in order to store all the I and Q data in FIFO (First In First Out storage device). The test system divides the IQCLK signal into the four frequency divider with EPLD chip, stores the data into the EPLD chip, and finally sends I data and Q data into the FIFO memory (each rising edge of the clock sends 16bit data in FIFO) four times. This test system stores a 24 bit's data using two writing clocks which is IQ_wclk (the rising edge of effective) because the FIFO chip is 18 bit width, but the I and Q data is 24. In the chip of EPM7128, Store data is triggered by external signal. The specific sequence is shown in Fig. (**2**).

4. THE REALIZATION OF DATA TRANSMISSION

4.1. The State Machine of GPIF

The test system uses the USB interface between the test card and the host, because this system needs a large amount of high speed data. The test system chooses the Cypress Company's EZ-USB series FX2 chip (CY68013-128AC). The EZ-USB FX2 chip supports USB2.0 high-speed transmission, to achieve the maximum sustained throughput in USB 2.0 High-speed designs; EZ-USB FX2's GPIF (General Programmable Interface) provides a highly configurable and flexible glueless peripheral interface that allows the highest possible bandwidth to be achieved over the physical layer.

EZ-USB FX2 chip has a 8051 processor and a general General Programmable Interface (GPIF). It is very important for data transmission between FIFO and the host. This test

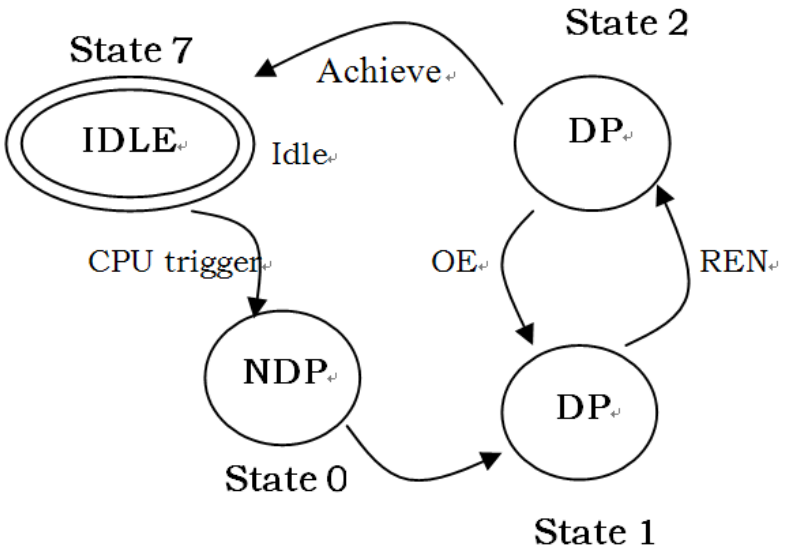

Fig. (3). State machine of GPIF.

system have several important signals, including: REN, OE, RCLK, IFCLK, RDY [5..0], CTL [5..0] *etc*.

In order to use the high speed mode of the FX2 chip, the design uses the state machine to achieve the FIFO read timing, state machine is shown in Fig. (**3**).

This test system uses 48MHz IFCLK signal for the read clock signal of FIFO chip, connects CTL [1] signal with REN signal, connects CTL [2] signal with OE signal, and then connects RDY[0] signal and RDY [1] signal with empty and full flags (EF and FF) of the FIFO chip respectively. When the CPU is triggered, the state machine becomes S7 (Idle) into S0 state, S1 and S2 state are the main loop, and S1 state produces the REN signal. The data can be sent to the data Bus one clock cycle later since the REN signal of FIFO is available. When the OE signal is available in the S2 state, the data on the data Bus can be sent to the FIFO chip's memory. When TC counter counts to 0, state machine converts S2 state into S7 state (Idle). A normal OUT request packet sent will repeatedly call the state machine (TC value is set to 512 bytes).

4.2. The Program Design

The MCU (Single chip microcomputer) of this test system is CY68013, which completes the host command. In the read operation, MCU executes the state machine, produces the FIFO read time sequence, and sends the large quantities data of FIFO chip into the host by Bulk(batch) transmission mode of the USB 2.0.

Firmware program flow diagram is shown in Fig. (**4**). The firmware program is responsible for initializing the hardware unit and reset the device. When the equipment is powered, the driver of the host downloads the firmware to the on-chip RAM, which is named enumerate. In the test system, the transmission of data is in Bulk mode. In the USB endpoint, it uses the EP2 (Packet Size 512,4X buffer) for the IN package and EP6 (Packet Size 512, 4X buffer) for the OUT package, which the two endpoints provide a large capacity FIFO, which can be used for high speed transmission.

The System's driver is programed by WindowsXP DDK, the driver connects the test card and the host. When the driver is loaded into the operation system, system loads the EZ-loader for the first time, and begins the Enumeration operation, and then the EZ-loader loads the firmware program in the system. This process is the second enumeration.

The Applications is programmed by using Visual C ++ and Matlab mixed programming, and it is responsible for receiving and analyzing the real-time data, displaying the results. The application program can analyse the ADC performance, which includes the signal to noise ratio - SNR, total harmonic distortion - THD, signal and noise and distortion ratio - SINAD, and spurious free dynamic range – SFDR. In the analysis process, calculate the amplitude spectrum using the Fast Fourier Transform Algorithm (FFT). The minimum spectrum length of M is 65536; it can also display ADC waveform.

The method of I/Q signal performance analysis is: it has to obtain the M sampling points (sequence, continuous, software selectable); the original data must be processed by window-adding function; and this procedure is very useful for the non-coherent sampling signal. It is not required to use the window-adding function for the coherent sampling signal. It can take the sum of square of the power spectrum of real/ imaginary, acquired through the results of FFT. Then, the amplitude spectrum can be taken by making the power spectrum integral to square root. The final result will be normalization.

In addition, this test system can help analyze the spectrum, by separating the signal, the harmonic wave, the cross modulation wave, the noise and the DC signal. This test system can also calculate the signal, noise, harmonic

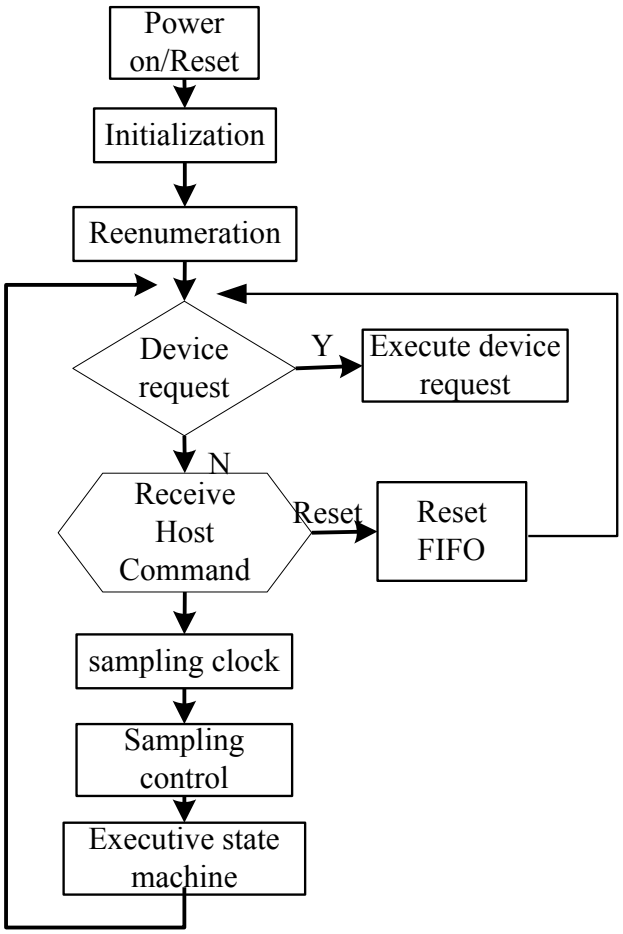

Fig. (4). Firmware program.

and the power of cross modulation wave. It can also calculate the amplitude consistency error, phase error, and the power calculation error.

CONCLUSION

Radar digital IF is the most important part of the radar system, whose performance significantly directly affects the performance of the radar digital signal process system. This paper introduces a digital IF test system design based on the USB interface, and introduces the main technology of the radar digital IF test system. At present, the design has been successfully applied to the digital IF testing, debugging, and has achieved good results.

ABOUT THE AUTHORS

First Author Han Bin, Associate professor of Chengdu University of Information Technology, Master. The author's major is Network Engineering and Computer interface technology. Two papers are received by EI and two patents had been published.

CONFLICT OF INTEREST

The author confirms that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

This work is supported by National Natural Science Foundation of P. R. China (61461046, 81260525), Higher School in Gansu Province Basic Scientific Research Expenses (2050205), Natural Science Foundation of Gansu Province (1010RJZE028) and Tianshui youth scientific and technological support projects (TSK1201).

REFERENCES

[1] J.W. Choi, N. I. Cho, "Suppression of nanow-band interference in DS-Spread spectrum systems using adaptive IIR notch filter", *Signal Processing*, vol. 82, pp. 2003-2013, 2002.

[2] N.I. Cho, S.U. Lee, "On the adaptive lattice notch filter for the detection of sinusoids", *IEEE Transactions on Circuits System*, vol. 40, no. 7, pp. 405-416, 1993.

[3] J. Fudge, M. Legako, C. Sehreiner, "An approach to efficient wide-band digital down conversion[C]," In: *IEEE Proceedings of IC SPAT*", Toronto, 1998, pp. 713-717.

[4] W. Ji-bin, M. Xian-de, J. Zhen-yuan, "Realization of quadrature coherent detection by direct sampling of IF signal", *Journal of Harbin Institute of Technology*, vol. 33, no. 1, pp. 116-119, 2001.

[5] D. M. Akos, "Direct bandpass sampling of multiple distinct rf signals", *IEEE Transactions on Communication,* vol. 47, no. 7, pp. 983-988, 1999.

[6] K. Gerlach, M. J. Steiner, "An adaptive matched filter that compensates for I, Q mismatch errors", *IEEE Transations on Signal Processing*, vol. 45, no. 12, pp. 3104-3107, 1997

[7] I. H. Sohn, E. R. Jeong, Y. H. Lee, "Data-aided approach to I/Q mismatch and DC offset compensation in communication receivers", *IEEE Communication Letters,* vol. 6, no. 12, pp. 547-549, 2002.

[8] C. Cheng, K. K. Parhi, "Low-cost parallel FIR filter structure with 2-stage parallelism", *IEEE Transcations on Circuits and System I: Fundamental Theory and Applications*, vol. 54, no. 2, pp. 280-290, 2007.

Received: September 16, 2014 Revised: December 23, 2014 Accepted: December 31, 2014