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A New Optical Design of Worm Precision Detection Based on FPGA

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Abstract: This paper proposes a design of detecting system on new optical worm drive precision based on Field Programmable Gate Array(FPGA). By taking Verilog HDL as hardware description language to design, this platform adopts FPGA to process grating scale fastened on the check-waiting worm pair at the gauge chassis and the optical angle encoding signal synchronously. Subdivision technology is used to improve resolution of measuring grating and precision and scalable MC8051 IP core is embedded to control reading signal preprocessing data. By serial communication, the coordinate size and error precision are both displayed and analyzed on the virtual apparatus Labview software as well as data statistics information during driving process. The experimental results verify that the designed optical worm precision detecting system could meet the requirements of precision and ensure the products' machining quality.

Keywords: FPGA, MC 8051 IP core, Driving Detection, Frequency Division Technology

1. INTRODUCTION

As a consequence of the fact that worm drive is widely applied in precision machine tool, motor control, machining and other industrial actual production, especially for high-precision well-stable condition, it is necessary to detect the mass of worm and drive error in real time. The conventional detecting system design tends to adopt digital gate circuit to set up or Microchip Unit(MCU) to control peripheral counting circuit to fulfill the system design [1, 2]. However, this kind of method uses excessive circuit separators, hence there exists to be some problems including decreasing stability for long-time operating and poor flexibility when updated.

The worm precision detecting system that this paper proposes is that, by installing optical grating transducer on the alternating-axis drive platform which consists of flexibility-tooth standard worm gear and check-waiting ZA worm, utilizing high-reliable Field Programmable Gate Array(FPGA) with an embedded in MC8051 IP core to build system on chip to test new method to accomplish data collection and analysis on drive accuracy. With the rapid development of electronic design technology, the complexity of FPGA that users demand is increasingly high and the function with which it is equipped is much more, chips are evolving towards to miniaturization. Step by step, they become the ideal choice for complex digital hardware circuit design.

2. DESIGN SCHEME

Except for mechanical drive components, the whole testing system is mainly composed of incremental optical grating sensor module, signal processing module inside FPGA chip and upper computer that undertakes display, control and memory function. The system structure block diagram is shown in Fig. (**1**).

Signal detecting transmission takes use of grating scale and angular encoder to output the angle value that worm gear rotates and position information of center distance of worm auxiliary drive [3]. The system adopts Cyclonell series EP2C8Q208C8N from Altera company as core processing chip to accomplish preprocessing multi-channel photoelectric encoder signals. With the help of MC8051, through software programming, data conversion and serial transmission are achieved. Then, by serial communication way, the virtual instrument in Labview on the upper computer receives and processes data to realize data and graph display as well as analytic statistics etc. The peripheral circuit mainly involves FPGA power supply voltage-stabilizing circuit, clock crystal oscillator circuit and various kinds of interface circuit design. This system design is based on FPGA multi-channel optical worm quality precision testing analyzer. It not only meets with the requirement of actual industrial machining and detection but also improves data processing speed and detecting reliability.

3. SYSTEM HARDWARE CIRCUIT DESIGN

3.1. Optical Sense and Interface Circuit

The optical rotary encoder and grating scale that this design uses belong to incremental angle encoder [4]. According to the axial rotary variable and the amount of movement between the unmoving scale fastened on the gauge chassis and moving scale, the rotary angle and the length of center distance are calculated by referring sense resolution through FGPA counts the amount of pulse signals synchronously. The incremental optical sensor has three output signals. They are phase A, B, C and Z signals respectively. The phase A

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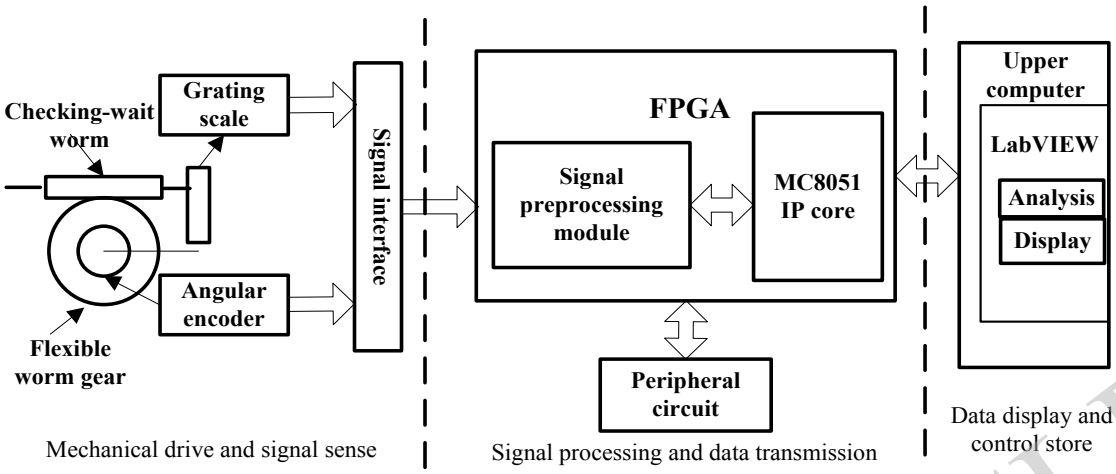


Fig. (1). The whole system block diagram.

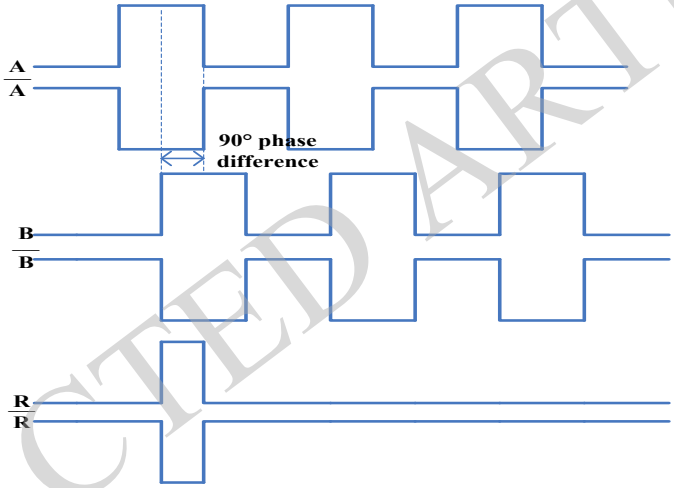


Fig. (2). EIA422 output signals.

and B signals are used to output the moving distance of moving scale and direction information. The Z signal outputs the two endpoints and midpoints information where moving scale is located on the grating scale. In the system, optical rotary encoder and grating scale compose digital grating sense elements which are installed on the gauge chassis [5, 6]. Its sense revolution is 360°/1024=0.35° and 0.01mm.

The incremental grating output signal is divided into two modes including TTL and EIA422A. The EIA422A output line adopts differential equation. Although its costs a lot, it could eliminate common-mode interference of communication signal. Moreover, it has superior communicating quality and appears regnant regarding transmission distance. The EIA422A signal output mode is shown in Fig. (**2**). The MC3486N differential receiver produced by TI compounds differential signals and finally outputs two-channel square signals which differ 90° each other. They are used to convert differential signals to single-ended TTL signals that could be recognized by FPGA and are beneficial to signal preprocessing directly. The principle of signal interface circuit is shown in Fig. (**3**).

3.2. FPGA Logic Design and Simulation

3.2.1. The System Top Design

The design of FPGA internal chip logic is the main part of the whole system. It mainly consists of signal preprocessing module and embedded MC8051 core transplant module. The signal preprocessing module includes signal smoothing, frequency multiplication and subdivision, sensing and recognition, reversible count, synchronous latch output. The MC8051 core transplant module replace the conventional MCU's function, realizing module timing control,

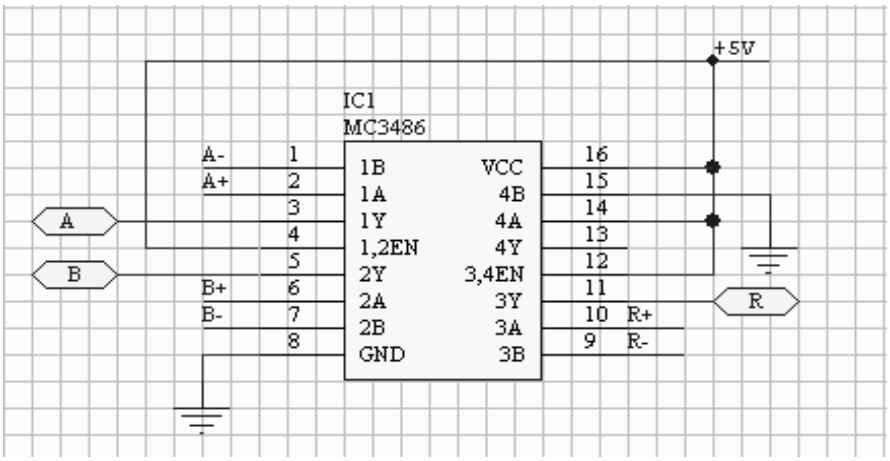


Fig. (3). The principle of signal interface circuit.

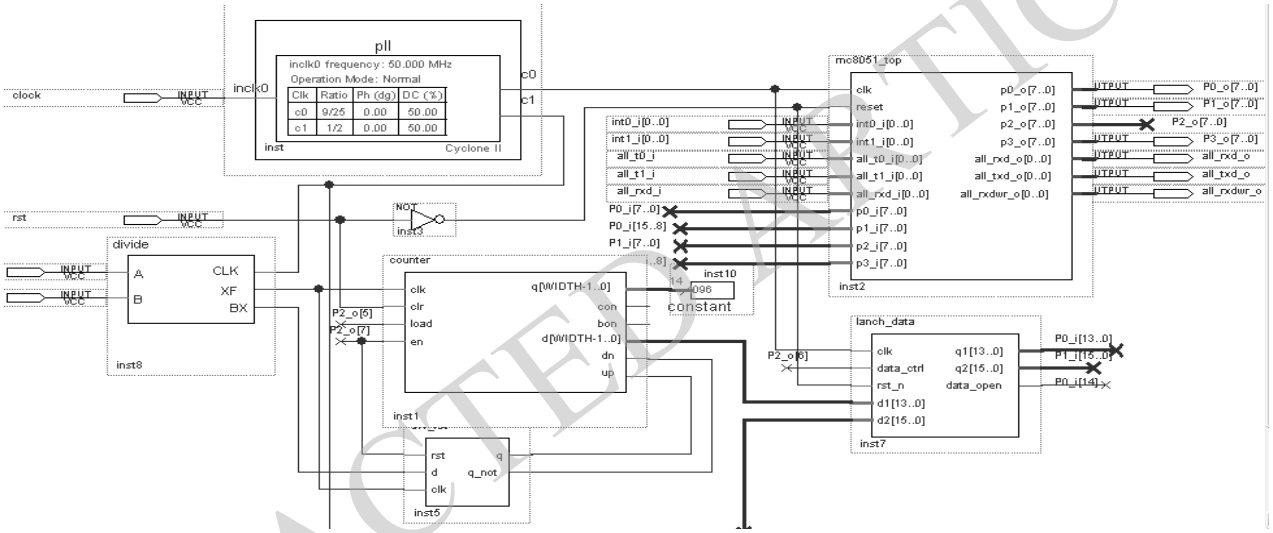


Fig. (4). The system top stereogram.

serial port and communication output and so on. Signal smoothing operation adopts the method of eliminating shake which carries on digital smoothing on the input signal from optical angle encoder. The eliminating width is less than noise signal of sample clock. The Fig. (**4**) shows each logic functional module in top stereogram.

3.2.2. Frequency Multiplication and Subdivision, Sensing and Recognition Module

The sensing and subdivision module is the main logic timing sequence inside FPGA in order to increase the measuring precision and resolution, As the A and B signals which are processed by interface circuit are perpendicular square-wave signal. In order to make the measuring precision of grating scale and angle encoder meet the request of system design accuracy, this project adopts four-times frequency multiplication and subdivision as shown in Fig. (**5**). Its logic idea is to realize producing 4 valid pulses in a period that grating counts. They are divided by the electrical levels in phase A and B. For example, when phase A is ahead of phase B with 90°, the combination of A and B electrical level could appear four states 00-10-11-01. When phase B is ahead of phase A with 90°, the four states will also appear. According to the two above states, the direction could be recognized [7]. The simulation waveforms of ttis frequency multiplication and subdivision function is shown in Fig. (**6**).

3.2.3. The Latch Module

In order to endure that the two data routes from encoder and grating scale could capture synchronously, add a latch to control logically between reversible counter and MC8051 IP core to guarantee the synchronism of the two data routes. As MCU and latch are in different time domain, when Verilog is in logic design, an asynchronous single–bit synchronizer is necessary, avoiding metastable state. In order to verify the module's feasibility, it is confirmed by simulation and its time sequence figure is as Fig. (**7**) shows.

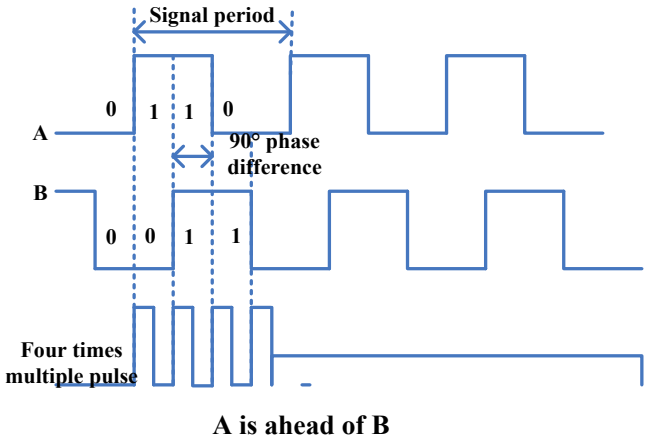


Fig. (5). The principle of four times subdivision.

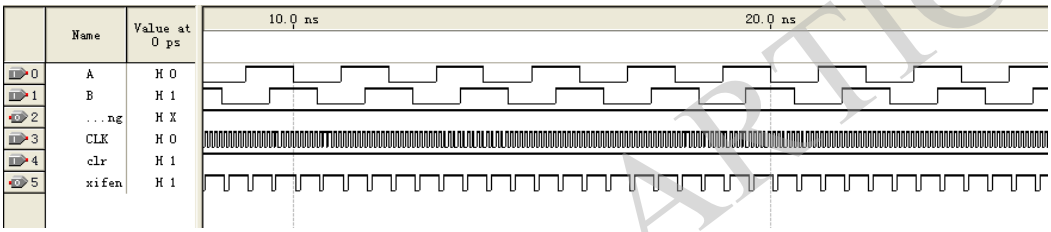


Fig. (6). The simulation waveform of subdivision.

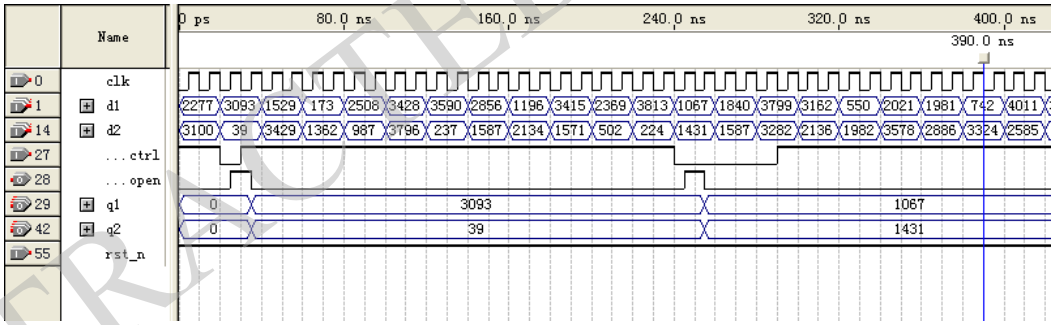


Fig. (7). The simulation result of asynchronous latch module.

4. THE SYSTEM SOFTWARE SESIGN

The software design mainly consists of MCU data processing program written by C language and Labview graphical human-computer interface design in upper computer, in which the real-time receiving when collecting data, controlling and displaying are the essential part of the whole software design.

4.1. MCU Data Processing Program Design

Firstly, inside MCU, the corresponding registers, serial port interrupts and peripheral modules are set initially. Then, the I/Os which are input by conterminal latch control and read the count value from signal preprocessing circuit. Data are combined and converted to be sent to LED display. Meanwhile, the program judges the two-route data with real-time whether it exceeds given range. According to the judgment, relevant counters control and process. If exceeding counting range, MCU enable counter module preset signal LOAD valid and makes it start to count from the reference position. During period that the main program displays and processes data, through serial port, MCU receives interrupt response from upper computer and sends request commands or suspends receiving commands at any time, then controls sending mark Flag_uart through interrupt response to realize data communication. The main program is in Fig. (**8**) as below.

4.2. The Receiving Program Design in Upper Computer

The upper computer program mainly achieves receiving the data from FPGA chip's serial port and start control.

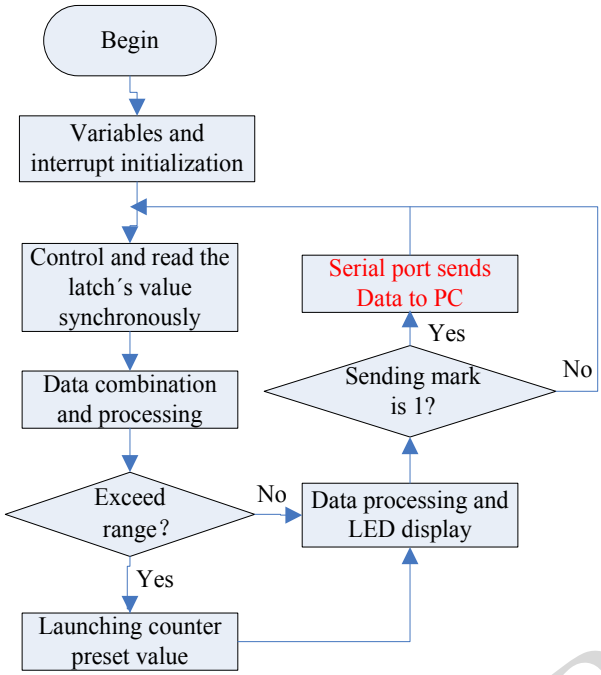
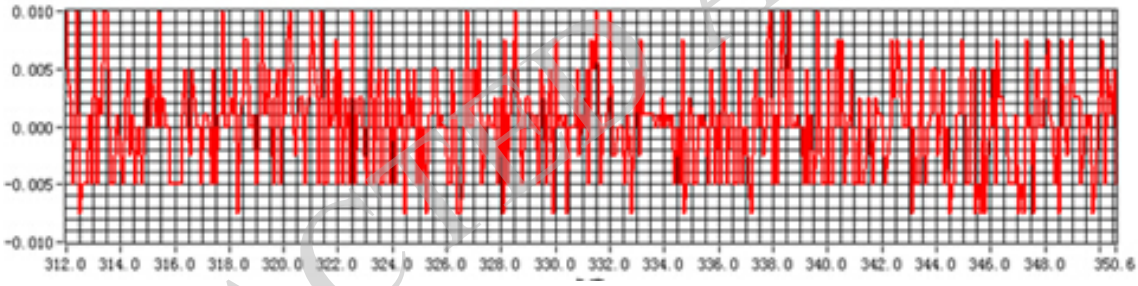
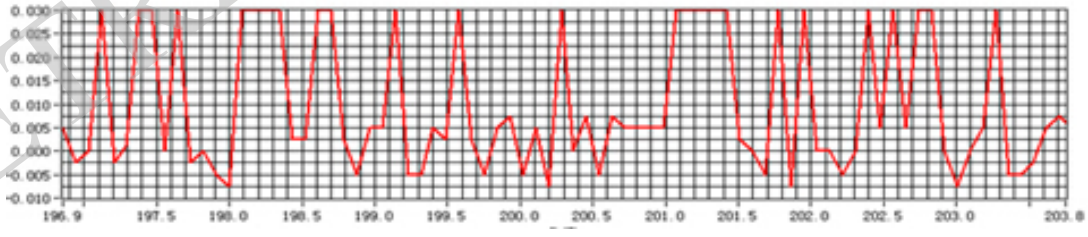


Fig. (8). The flow diagram of data processing.



(**a**) Normal record



(**b**) Abnormal record

Fig. (9). Worm test records.

Besides, it could show the error curve of center distance in real-time. It collects, analyzes and stores data to be read by data processing software. The system adopts Labview to write virtual apparatus program. Adopting Labview program design, programmer need not consider writing complex specialized drive programs but handle Labview to provide devices and functions [8]. Thus, the main effort is concentrated on the design of control and algorithm.

5. THE DETECTION VERIFICATION AND CONCLUSION

Meshing check-waiting worm and standard worm which are then put on the gauge chassis, rotate screw-driven plate to squeeze into equipped state. Therefore, the text devices are connected to hardware and human-computer interface is linked to software. According to the angle value and

indicating light shown by Labview, the current state of worm gear is estimated to ascertain whether forward or backward. Then DC motor could make sure its rotating state. The driven center distance error σ shown in 2-D figure coordinate is the absolute value of meshed center distance and theoretical center distance of worm gear pair in dynamic process which is used to express actual machining precision.

By measuring and calculating actual driving center distance error σ unremittingly, the alarm will ring and displays the worm is abnormal if exceeding the set reference value ∂. According to Fig. (**9b**), it could be discovered that substandard worm has already exceeded the set value(0.015mm) which could not satisfy the machining precision requirement. From the Fig. (**9a**), the maximum actual driving center distance error σ is 0.01mm which verifies the system's reliability and accuracy on error analysis. In this experimental test, the serial port communication is set as COM1, 9600bps, 8-bit Date bits, 1-bit stop bit without parity check bit and flow control.

The experimental results indicate that this paper proposes a design on multi-channel grating worm quality-detected and fast analytical system based on FPGA with embedded 8051 IP core. The method of design has simple structure and high integration level. Compared with conventional designing methods, it uses much less devices and is easy to preserve and upgrade. On the condition of ensuring the function of each part, the volume and power dissipation are both optimized. The simulation results also verify its feasibility. The practice shows that this system truncate developing cycle with simple hardware circuit, preferable real-time, stable test, extensible functions and so on.

CONFLICT OF INTEREST

The author confirms that this article content has no conflict of interest.

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Declared none.

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