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Development of automotive collision avoidance system based on intelligent control

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ABSTRACT: The software system is 16-bit microcontroller as the control core, the Ultrasonic signal by the signal acquisition input to the MCU, the MCU achieves the motor speed control for signal processing. A infrared sensor is used to measure speed and makes motor control more precise and stable .A small motor is installed at the car throttle，and by collecting information the microcontroller can control the opening of the throttle, thus avoiding the traditional mechanical throttle human operator errors and wasteful. By a suitable algorithm, intelligent speed control system has been studied in the PWM module program, ECT module program, PIT module program, PLL module program, and the intelligent system studied in the throttle, the entire software is completed in the end. The results showed that the system is reliable in performance, has high resolution and an accurate control, greatly preventing the car collision from the car ,and protecting the driver's personal safety.

Keyword: Automotive collision avoidance Intelligent control Ultrasonic signal Infrared sensor Speed Control

Introduction

According to the state administration of work safety, 110000 people lose their lives because of traffic accidents in China each year, making China one of the world leaders in terms of traffic accident-related deaths. Data were taken from the Transportation and Communities year book of China, road traffic death rate increased by 95 percent from 1985 to 2005 (Barboza, 2011). How could this happen? What are the main causes of this and what could Chinese people do towards this? Here are two traffic accidents in China and the USA.

The road traffic safety is very grim. China form. Statistics show that the number of fatal traffic accidents in China are each of nearly 100000, accounting for one point five percent of the total death toll. The seventh cause of death. The minutes died under the wheel. Every minute a person dies because of traffic accidents and disability.Each year caused by traffic accidents economy loses a lot of people and reaches hundreds of billion.

In recent years ,along with the increasing of all kinds of vehicles,traffic accidents continue to occur. According to relevant statistics, China has 1.9% of the world’s automobile, traffic accidents have accounted for15% of the world, each year the number of killed in traffic accidents is more than100000,.

In the highest in the world.Traffic accidents continue to occur,caused a great threat to people’s life and property safety and social order and stability,and has become a serious social problem.

Therefore, the safe driving cars will become one of the main causes of family stability . Real life incidents have occurred when the car rear-ended, and so he mistakenly put his foot on the accelerator instead of the brake causing a fatal car crash tragedy which deeply touched my heart .With especially microcontroller development of electronic technology, you can make the car towards a more intelligent move. Currently the domestic cars have only seat belts and airbags, the airbag is not only costly, but also has a large space, and the safety factor is not high. The project researched an intelligent vehicle collision avoidance system ,aimed to detect distance between the two vehicles.According to the distance it can control the back car's speed. The back car automatically puts brakes from the vehicle and a short distance is from the front vehicle. The research developed low-cost, high performance, small footprint, high safety factor, market prospects, and it is greater significance to promote China's actual level of the automotive industry. The system uses software and hardware combination of methods, modular and multi-use characteristics. By this token,the project is very broad in market prospects.

The overall block diagram of the software

The overall block diagram of software design is as follows:

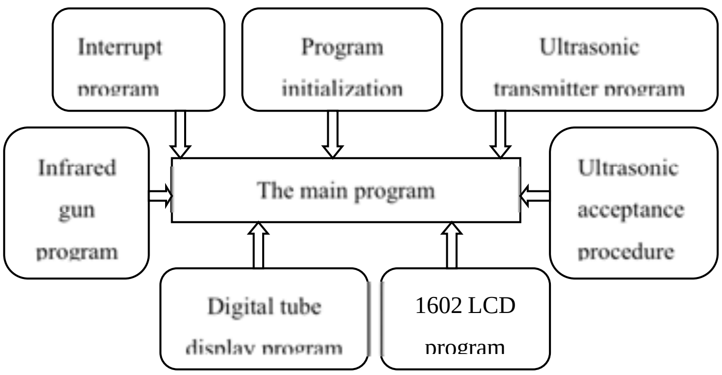

Fig 1 Software design diagram

This program core is based on MC9S12xs128, when the ultrasonic signal acquires, the program has returned and interrupts the process, and controles the DC motor.

Program flow chart:

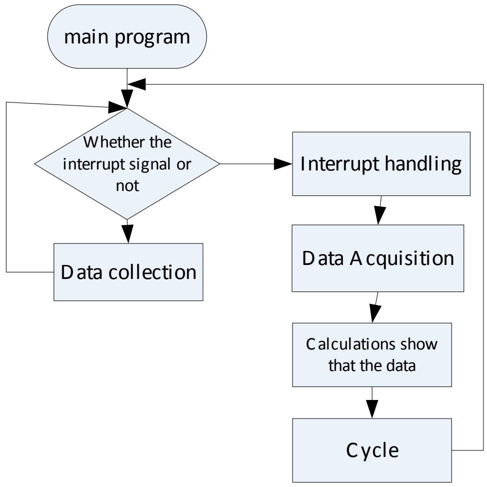

Fig 2 Software design flow

PWM module program

The PWM modulation wave has eight output channels, each output channel can be independently output. Each output channel has a precise counter (calculated pulse number), a cycle of control registers and two alternative clock source.

Each PWM output channel can modulate the waveform changes of the duty cycle from 0 to 100% of

The main features of the PWM

The PWM has eight independent output channels, each output channel has a precise counter; PWM output enable channel can be controlled by programming; Flip control PWM output waveform can be programmed to achieve; cycle and pulse width can be double-buffered.When the channel is turned off or PWM counter is 0, it can only work by the change of the cycles pulse width; and has 8 bytes or 16 bytes of channel protocol. There are four clock source options (A, SA, B, SB). they provide a wide range of frequencies.

Related calculations

1) Calculate the clock

The clock SA is generated by PWMSCLA register settings to the A clock frequency.

Clock SA=Clock A/(2*PWMSCLA);

The clock SB is generated by PWMSCLB register settings to B clock frequency.

Clock SB = Clock B / (2*PWMSCLB);

2) Period calculation

①When CAEx=0, that were left linear output:

PWMx cycle=channel clock cycle * PWMPERx;

②When CAEx=1, namely, the center-aligned output: PWMx cycle=channel clock cycle*(2* PWMPERx);

3) Calculation of duty

When PPOL=0: Duty=[(PWMPERx-PWMDTYx)/PWMPERx]*100%;

When PPOL=1:

Duty=(PWMDTYx/ PWMPERx)*100% ；

PWM initialization procedure

PWME_PWME2=0x00; // Disable PWM
PWMPRCLK=0x33; // 0011 0011 A=B=24M/8=3M
PWMSCLA=150; // SA=A/2/150=10k
WMSCLB=15; // SB=B/2/15 =100k
PWMCLK_PCLK2=1; // PWM3-----SB
PWMPOL_PPOL2=1; // Duty=High Time
PWMCAE_CAE2=0; // Left-aligned
PWMCTL=0x00; // no concatenation
PWMPER2=100; // Frequency=SB/100=1K PPWMDTY2=0; // Duty cycle = duty
PWME_PWME2=1; // Enable PWM

ECT module program

ECT feature

The ETC has four IC channels . It can set 16 holding registers for buffering to capture the results and have four 8 pulse accumulator, four 8 holding registers associated with the buffer IC Channel; four eight-channel pulse accumulator can be cascaded and forms two 16 pulse accumulator; four scaler 16 modulo counter is decremented; four optional delay counter is used to enhance the anti-jamming capability; only supports 16 access in IP bus.

ECT operating mode

Stop: Since the clock is stopped, timers and counters are closed; freeze: timers and counters are kept running until TSFRZ bit of TSCR ($06) is set to 1; wait: Counter keeps running until TSWAI bit of TSCR ($06) is set 1; normal: timers and counters are kept running until TEN-bit of TSCR ($06) and MCEN bit of MCCTL ($26)is cleared respectively.

ECT composition and mode of operation

Two pairs of 8 bite pulse accumulator can also be cascaded to form a 16-bit pulse accumulator PACA, PACB. 16 decreasing modulus counter (MDC) is the additional ECT, it is not only a functional timer with independent programmable scaler, auto-reload and interrupt capability, but also provided transmission timing control signal for the IC, PAI register to keep registers. Whenever the MDC is back to 0, the ETC controled IC and PAI register ‘s content to the respective buffer register in a given period of time. Of course, MDC is used as a timer interrupting the function of independent clock reference.

Timer and A/D counter perational state

Stop (STOP): Because PCLK and ECLK have stopped,timer and A/D counter closed;
debug mode (BDM): As long as does not meet TSBCK=1, timer keeps running;
interrupt wait (WAIT): As long as does not meet TSWAI=1, counter keeps running;
normal (Normal): As long as does not meet TEN=0 and MCEN (MCCTL in)=0, the timer keeps

running;

ban (TEN=0): timers and MDC stop,

ECLK/64 clock is disabled;

ban (PAEN=0): All pulse accumulator operation is stopped, but the register can be accessed;

MCEN: 0: modulo counter stop;

PAEN: 1,16-bit pulse accumulator a activation;

PAEN: 0,8-bit pulse accumulator 3 and 2 can be activated;

PBEN: 1,16-bit pulse accumulator B activation;

PBEN: 0,8-bit pulse accumulator 1 and 0 can be activated.

ECT initialization procedure

TIOS=0xFE; // Set input capture channel PT0

TCTL4=TCTL4_EDG0A_MASK|TCTL4_EDG0B_MASK; // PT0 capture rising edge and falling edge

TSCR2=0x87; // Timer overflow interrupt enable, divided by 128

TIE=0x01; // Open PT0 interrupt

TSCR1=TSCR1_TEN_MASK; // Timer Enable

PIT module program

PIT is a 24 timer array, peripheral modules can be used to trigger can cause periodic interrupt. Two micro-timer is 8-bit micro Timer0 and micro timer1; four is 16-bit timers Timer0, Timer1, Timer2, Timer3.

Four kinds of operation modes: run mode, basic modes of operation; wait mode, PIT mode of operation by PITSWAI of PITCFLMT register control; stop mode,the full stop or pseudo stop mode, PIT stop s running; According to freeze mode, PIT mode of operation is by PITFRZ of PITCFLMT register control.

PIT Features

When 16-bit and 8-bit counters are reduced to 0, PITLD register is reloaded. The corresponding timeout flag of the PTF bit of PITTF is set to 1. Timeout period is a function of the PITLD ,PITMTLD and fBUS.

time-out period=（PITMTLD+1）*(PITLD+1)/fBUS;

40MHz bus clock, the maximum timing period is equal to（255+1）*（65535+1）/25ns = 419.43ms.

PIT interrupt interface

Every timeout event can trigger an interrupt request, and has a separate PINTE bit to achieve this function for each timing channel. When PITNTE is set 1, appropriate PTF of PITTF timeout flag bit is set to 1, it will request an interrupt service. PTF can be cleared by writing a 1 to the corresponding bit manually.

PIT hardware trigger

PIT module contains four hardware trigger signals in PITTRIG [3:0], each timing channel has one. These signals can be connected to Soc module and is used to control peripheral devices, such as cycle

ATD conversion; whenever a timing channel arrives, the corresponding PTF bit is set to 1, and the trigger signal PITTRIG trigger a rising edge.

PIT initialization and shutdown

The PITE bit is set to 1 before initialize all registers, the registers may be written in any order before PITE is set. When PITCE, PITINTE, PITE is cleared, the corresponding PIT interrupt flag bit is cleared. Suppose there is a queue of PIT interrupt requests, a spurious interrupt may be generated. There are two strategies to avoid this spurious interrupt:

1) Only in the ISR (interrupt service routine) Reset PIT interrupts flag when entering the ISR, CCR in the I mask flag is set automatically. I mask flag should not be cleared before the PIT interrupt flag.

2) After I mask is set using SEI instruction, PIT interrupt flag can be cleared. Then use the CLI command to re-enable interrupts.

A flag can be cleared by writing 1, you want to use to store instructions or directives to write 1 in the determined position (STRORE and MOVE), do not use the BSET instruction, and any C language statements may be compiled into BSET instruction do not use, "BSET flag_register, #mask", can not be used to clear the flag, because BSET is readable . According to writable and modify instruction, BSET instruction can operate or operator the value of flag_register and mask bit after the or operator values return, BSET will be cleared of all flags before the set.

PIT initialization procedure

```
  PITCFLMT = 0x00; //close PIT
PITCE = PITCE_PCE0_MASK;
// Open the timer channel 0
PITMUX = 0x00;
 //Timing channel 0 using micro counter 0
PITINTE = PITINTE_PINTE0_MASK;
 // Enable timing channel 0
  PITMTLD0 = 80-1; // Set micro counter load register 0
  PITLD0 = 1000-1; // Set 16-bit counter load register
  PITCFLMT = PITCFLMT_PITE_MASK; // Enable PIT
```

PLL module program

PLL: Phase synchronization logic. The closed loop is an automatic frequency (phase) adjustment process,so called ring. Phase-locked loop is divided by two kinds of analog phase-locked loop and digital phase-lockedloop.

Phase-locked loop line was originally used to improve the television receiver and frame synchronization to improve the anti-jamming capability. In electronic instrumentation, Phase-locked loop plays an important role in PLL frequency synthesizer,phase meter and other equipment. PLL applications currently focus on the following three aspects: firstly, signal modulation and demodulation; secondly, frequency modulation and demodulation; thirdly, signal frequency synthesizer circuit.

Analog phase-locked loop and digital phase-locked loop

The analog phase-locked loop consists mainly of extraction circuit, voltage controlled oscillators, phase by phase comparator reference and the control circuit etc. The voltage controlled oscillator output frequency is very close to the needs of equal amplitude signals, It compared with a reference signal from the phase extraction circuit extracting the signal and fed to the phase comparator at the same time . The voltage controlled oscillator frequency is reduced in absolute error continuously changing direction by comparison becoming error, to achieve phase lock, so as to achieve synchronization.The divider output signal frequency is very close to the desired frequency, compare the divider output signal with the signal phase of the reference signals in a phase comparator simultaneously,comparing the results are shown when the local frequency is higher in complement wipe and gate erases one input divider pulses The local oscillation frequency is decreased;on the contrary, if the frequency low shows that the local time of a pulse is inserted between the input terminal of the two input pulse divider, the local oscillation frequency is increased, so as to achieve synchronization.

PLL initialization procedure

```
CLKSEL=0X00;


PLLCTL_PLLON=1;// OPEN PLL
SYNR=0xc0 | 0x09;
   // VCOFRQ[7:6];SYNDIV[5:0]
  // fVCO= 2*fOSC*(SYNDIV + 1)/(REFDIV + 1)
  // fPLL= fVCO/(2*POSTDIV)
  // fBUS= fPLL/2
  // VCOCLK Frequency Ranges    VCOFRQ[7:6]
REFDV=0x80 | 0x01;
  // REFFRQ[7:6];REFDIV[5:0]
 POSTDIV=0x00;
   asm(nop);
_asm(nop);
while(!(CRGFLG_LOCK==1));
CLKSEL_PLLSEL =1;
```

Intelligent Throttle Circuit

Traditional electronic throttle controls are based on the judgment of the human brain, with uncertainty, the throttle opening is unstable, resulting in excessive oil consumption than the smart throttle (fuel ratio constant).

Electronic throttle obvious point is that you can use to replace the cable harness or lever mounted on the throttle side of a miniature motor, makes use of electric motor to drive the throttle opening. The so-called "line drive", to replace the original mechanical transmission mechanism.That intelligent Electronic throttle position adjusted throttle opening degree is sensored by the hand and is transmitted to the desired signal MC9S12xs128, Through the obtained data (torque and speed) analysing, so that the output signal of the drive motor adjusts the opening degree of the door and gas. Such as the engine is always in the best condition, greatly improved vehicle performance, improved driving comfort, reduces fuel consumption, reduced emissions of pollution; can meet environmental requirements in a better way.

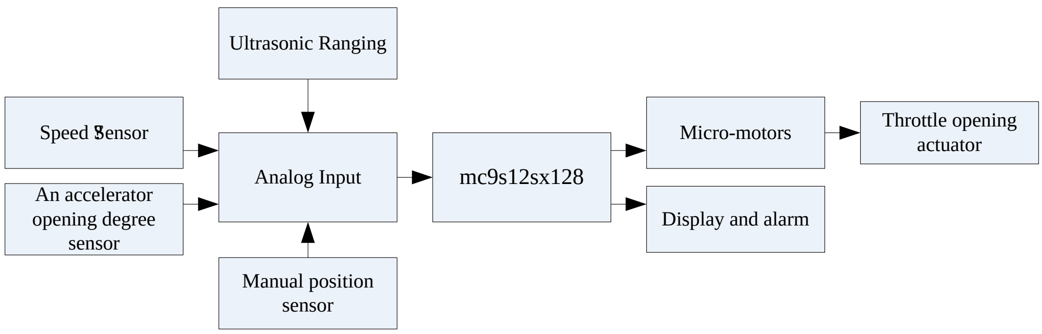

Fig3 Intelligent electronic throttle schematics

Conclusion

The research uses ultrasonic distance measurement principle, a safe judgment function, when the distance between the car and the obstacle is less than a setting safe distance, the system can sound an alarm, and with the

continuous shrinking closer, it is possible to gradually
slow down . This technology is a great innovation of modern vehicles, for automotive safety, energy produce more far-reaching significance.

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