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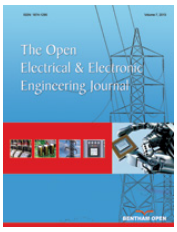

RESEARCH ARTICLE

A DC Voltage Control Strategy for Active Power Filter

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Abstract: Active Power Filter (APF) is capable of changing the size and frequency of harmonics as well as changes in reactive power compensation. It is important to control the stability of the DC-link capacitor voltage stability for it. For DC voltage controls of APF, there are two important achievements. First, it is indicated that the control of DC voltage directly affects the compensation performance of APF. Second, the value of DC voltage influences the power loss of APF. This paper firstly introduces the design of the DC voltage controller. Then the relationship between DC voltage and the power loss as well as the compensation performance of APF is analyzed. Finally, a new control scheme with a droop controller is developed to regulate DC voltage.

Keywords: Active Power Filter, DC-link voltage, Insulated gate bipolar transistors, Open-loop voltage, Sinusoidal pulse width modulation, Three-phase three-wire.

1. INTRODUCTION

For an Active Power Filter (APF), it is important to control the stability of the DC-link capacitor voltage stability. As mentioned in [1 - 4], the premise condition for APF working normally is that the DC-link voltage should be greater than the line voltage peak, and the minimum DC-link voltage in the linear modulation range is given. In [1, 2] the influence of DC-link voltage reference value (the grid phase voltage RMS) on the compensation performance of APF is analysed, and the general control scheme selected for DC voltage is further proposed in [5, 6]. Two important results related to DC voltage control of APF have been gotten [7 - 9]. First, it is indicated that the control of DC voltage directly affects the compensation performance of APF. Second, the value of DC voltage influences the power loss of APF.

Taken the three-phase three-wire APF as an example, this paper firstly introduces the design of the DC voltage controller [10 - 13]. Then the relationship between DC voltage and the power loss as well as the compensation performance of APF is analysed [14, 15]. Finally, a new control scheme with a droop controller is developed to regulate DC voltage [16].

2. THE DC SIDE VOLTAGE CONTROL OF APF

Fig. (**1**) shows the control scheme of three-phase three-wire APF. Here, U_{dc_ref} is the reference value of DC voltage, U_{dc} is the sampling value, I_{dcd} is a regulating signal that is the difference between U_{dc_ref} and U_{dc} through voltage regulator. And i_{dcd} is added to the *d*-axis component of the output current reference. In fact, the *d*-axis DC component i_{dcd}, which represents the fundamental frequency components of the active currents, causes the real power exchange between AC and DC side.

Before designing the voltage controller, the conversion factors from AC input current i_d`i_q to DC output current i_{dcd} must be known. According to the mathematical model of APF, it has $i_{dc}=1.5(S_d i_d+S_q i_q)$. Here, the relationship between

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AC and DC current is time-varying because of two variables S_d and S_q. To simplify the process and design it with thelinear method, it is believed that i_q has completed the transient process reaching to 0 before a large change on the DC voltage, in which the value of i_q equals 0 in steady state, and i_q changes slightly in a dynamic process due to the current closed-loop. Based on this, the d-axis block diagram of the voltage outer-loop control can be seen in Fig. (**2**)

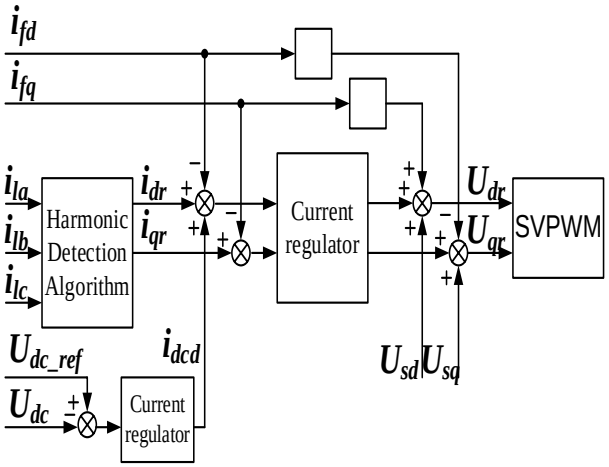

Fig. (1). The control scheme of three-phase three-wire APF.

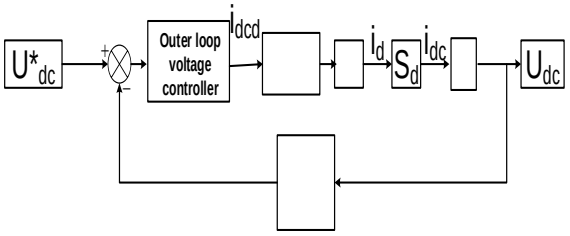

Fig. (2). Axis block diagram of the voltage.

Where $G_c(s)$ is the closed-loop transfer function of inner current, T_{vf} means the delay time constant of voltage feedback path (switching frequency is 9600*Hz*, or delay time is 104 *us*). K_{vf} means the amplification factor of the voltage feedback path (taking 1). K_{if} means the sampling coefficient of the output current (taking 16.384), and the capacitor C takes 20 *mF*.

Due to the second-order of the transfer function of current closed-loop $G_c(s)$, it is better to lower the order of $G_c(s)$ so as to make the synthesis of the voltage loop easier. The process is shown as follows:

The transfer function of the inner current control loop is:

$$G_c(s) = \frac{1}{2T_{sf}S + 1} \tag{1}$$

The open-loop transfer function without the controller is:

$$G_v(s) = \frac{K_{if}}{2T_{sf}S + 1} * \frac{K_{vf}}{T_{vf}S + 1} * S_d * \frac{3}{2CS} \tag{2}$$

Because T_{vf} and T_{sf} are time constant, so equation (2) can be simplified as bellow:

$$\left.\begin{aligned} G_{vc}(s) &= \frac{1.5K_{if}K_{vf}Sd / C}{S(T_vS + 1)} \\ Tv &= 2T_{sf} + T_{vf} \end{aligned}\right\} \tag{3}$$

The transfer function of PI controller is:

$$Gpi(s)=\frac{K_{vi}(\tau_v S+1)}{S} \tag{4}$$

Thus, the open-loop transfer function with PI controller is:

$$\left.\begin{aligned} G_{ve}(s)&=\frac{K(\tau_v S+1)}{S^2(T_v S+1)}\\ K&=1.5K_{vi}K_{if}K_{vf}S\ \ d/C \end{aligned}\right\} \tag{5}$$

From the analysis above, it can be seen that equation (5) is a typical type II system, the controller parameters can be designed according to Oscillation index method. The key point of the Oscillation index method is to select parameters according to the practical engineering requirements for the closed-loop relative resonance peak. Based on this, it can be ensured the system performance index does not exceed a specified value, *i.e.* the maximum overshoot is not greater than a certain limit value, the corresponding phase margin is the biggest, and the amplitude margin is the best, also the adjusting time is the shortest. Fig. (**3**) shows the Bode diagram of the open-loop voltage with PI controller.

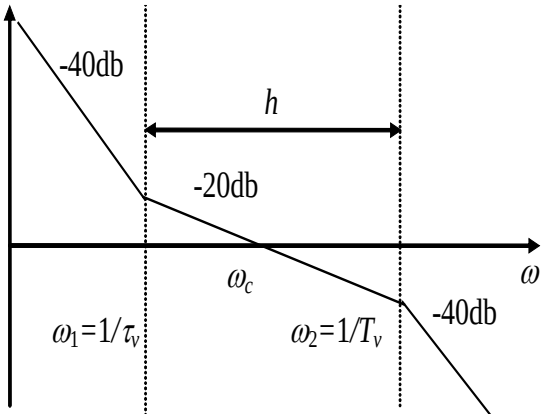

Fig. (3). Bode diagram of the open-loop voltage with PI controller.

From the Bode diagram in Fig. (**3**), a best fit between the two parameters can be found based on the minimum peak norm of amplitude-frequency characteristics in Oscillation index method. When the closed-loop resonant peak M_r reaches to the minimum, the relationship of each variable is obtained as:

$$\left.\begin{aligned} \frac{\omega_2}{\omega_c}&=\frac{2h}{h+1}\\ \frac{\omega_c}{\omega_1}&=\frac{h+1}{2}\\ M_r&=\frac{h+1}{h-1} \end{aligned}\right\} \tag{6}$$

The key to design the voltage loop is determining the bandwidth h. Practical experience shows that the width of medium-frequency h varies generally between 3 to 10. In addition, a larger h does no significant effects on decreasing M_r. When h=constant, it can be derived as:

$$\left.\begin{aligned} \tau_v&=\frac{h}{w_2}=hT_v\\ K&=\omega_1\omega_c=\omega_1^2\frac{h+1}{2}=\frac{h+1}{2h^2T_v^2} \end{aligned}\right\} \tag{7}$$

So the parameters of the voltage controller can be gotten.

$$Sd \subset [0, \sqrt{3}/3] \quad \text{h=5,K=693420}, \tau_v = 0.0021$$
$$K_{vi} = 1466, \tau_v = 1.3*10^{-3}$$

The PI controller of the voltage outer-loop is:

$$Gpi(s) = \frac{1.906s + 1466}{s} \tag{8}$$

3. THE INFLUENCE OF DC VOLTAGE ON POWER LOSS

The power loss of APF mainly includes the following two aspects: the switching loss of PWM inverter and the output inductor hysteresis loss, copper loss, *etc.*

The output current of APF is higher harmonics, and including some switching ripple current. In general, the switching frequency is much higher than that of the output current, so the output inductor hysteresis loss is mainly proportional to the size of the switching ripple current as well as the area surrounded by the magnetization curve of the magnetic material. When magnetic material with small magnetization curve area and high permeability, such as amorphous material, is selected, the output inductor hysteresis loss will be reduced to a relatively low percentage.

However, switching loss of PWM inverter actually contains IGBT switching loss, the diode reverse recovery loss, and the conduction loss of IGBT as well as the diode.

Furthermore, the IGBT conduction loss is proportional to the drop voltage and the flowing current, and the drop voltage increases with the flowing current. So it can be concluded that the conduction loss of IGBT increases as the APF output current rises. And this is also suitable to the diode conduction loss.

The IGBT switching loss includes turn-on and turn-off loss, and both the two components increases with DC voltage in case of the constant flowing current and switching frequency. It does also apply to the diode reverse recovery loss.

The main components of these losses mentioned above are IGBT switching loss and diode reverse recovery loss. With the constant switching frequency and output current, any increase/decrease in DC voltage causes a relative increase/decrease in the power loss of APF.

In addition, due to the complexity of the switching loss simulation, the relationship between DC voltage and the power loss of APF will be verified depending on experiments.

4. THE INFLUENCE OF DC VOLTAGE ON COMPENSATION PRECISION

Without considering the influence of current regulator and the error of harmonic extraction algorithm, the capability of compensating harmonic currents of nonlinear load is important to be considered in order to analyse the compensation performance of APF. Based upon the topology structure of APF and neglecting the inverter loss, according to equation (9), the output current of APF is relevant to the inductor drop voltage which can be easily obtained by a simple subtraction of the midpoint voltage of PWM inverter arms and the grid voltage.

$$\begin{cases} L\dfrac{di_{fa}}{dt} = U_{sa} - U_{fa} = U_{sa} - S_a U_{dc} - U_{NO} \\ L\dfrac{di_{fb}}{dt} = U_{sb} - U_{fb} = U_{sb} - S_b U_{dc} - U_{NO} \\ L\dfrac{di_{fc}}{dt} = U_{sc} - U_{fc} = U_{sc} - S_c U_{dc} - U_{NO} \end{cases} \tag{9}$$

In order to quantitatively analyse further, assuming the system is symmetrical, U_{sm} is the peak of the grid phase voltage, *and* ω is the power system angular velocity. And the three-phase source voltage can be defined as:

$$\begin{aligned} u_{sa} &= U_{sm}\cos(\omega t) \\ u_{sb} &= U_{sm}\cos(\omega t - 2\pi/3) \\ u_{sc} &= U_{sm}\cos(\omega t + 2\pi/3) \end{aligned} \tag{10}$$

Suppose the load is the three-phase uncontrolled rectifier with LR connection. According to the characteristic of the nonlinear load, it only exists $6n\pm1$ harmonic orders in the load current, where $6n+1$ is the positive sequence component, and $6n-1$ is the negative one. Without considering the influence of current regulator and the error of harmonic extraction algorithm, the APF output current and the PWM inverter output voltage can be established as bellow:

$$\begin{cases} i_{fa} = I_{f1m}\cos(\omega t + \theta_1) + \sum_{k=6n-1} I_{fkm}\cos(k\omega t + \theta_k) \\ \quad + \sum_{l=6n+1} I_{flm}\cos(l\omega t + \theta_l) \\ i_{fb} = I_{f1m}\cos\left(\omega t + \theta_1 - \frac{2\pi}{3}\right) + \sum_{k=6n-1} I_{fkm}\cos\left(k\omega t + \theta_k + \frac{2\pi}{3}\right) \\ \quad + \sum_{l=6n+1} I_{flm}\cos\left(l\omega t + \theta_l - \frac{2\pi}{3}\right) \\ i_{fc} = I_{f1m}\cos\left(\omega t + \theta_1 + \frac{2\pi}{3}\right) + \sum_{k=6n-1} I_{fkm}\cos\left(k\omega t + \theta_k - \frac{2\pi}{3}\right) \\ \quad + \sum_{l=6n+1} I_{flm}\cos\left(l\omega t + \theta_l + \frac{2\pi}{3}\right) \end{cases} \tag{11}$$

$$\begin{cases} u_{fa} = U_{f1m}\cos(\omega t + \varphi_1) + \sum_{k=6n-1} U_{fkm}\cos(k\omega t + \varphi_k) \\ \quad + \sum_{l=6n+1} U_{flm}\cos(l\omega t + \varphi_l) \\ u_{fb} = U_{f1m}\cos\left(\omega t + \varphi_1 - \frac{2\pi}{3}\right) + \sum_{k=6n-1} U_{fkm}\cos\left(k\omega t + \varphi_k + \frac{2\pi}{3}\right) \\ \quad + \sum_{l=6n+1} U_{flm}\cos\left(l\omega t + \varphi_l - \frac{2\pi}{3}\right) \\ u_{fc} = U_{f1m}\cos\left(\omega t + \varphi_1 + \frac{2\pi}{3}\right) + \sum_{k=6n-1} U_{fkm}\cos\left(k\omega t + \varphi_k - \frac{2\pi}{3}\right) \\ \quad + \sum_{l=6n+1} U_{flm}\cos\left(l\omega t + \varphi_l + \frac{2\pi}{3}\right) \end{cases} \tag{12}$$

Here, I_{f1m} is the peak of APF output fundamental current, U_{f1m} is the peak of PWM inverter output fundamental voltage, I_{fkm} and I_{flm} mean the peak of APF output the *k-th* and *l-th* harmonic currents respectively, U_{fkm} and U_{flm} represent the peak of PWM inverter output the *k-th* and *l-th* harmonic voltages respectively, θ and φ signify the initial phase angle of each order component.

According to the definition of Park transform, a space vector synthesized by any three-phase variables x_a`x_b and x_c can be illustrated mathematically as:

$$\overrightarrow{X} = \frac{2}{3}\left(x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{-j\frac{2\pi}{3}}\right) \tag{13}$$

Then equations (4-1) can be transfer to equation (14):

$$L\frac{d\overrightarrow{i_f}}{dt} = \overrightarrow{u_f} - \overrightarrow{u_s} \tag{14}$$

Substitute equations (10) ` (11) ` (12) into equations (13) ` (14), we can get:

$$j\omega LI_{f1m}e^{j(\omega t+\theta_1)}-\sum_{k=6n-1}jk\omega LI_{fkm}e^{-j(k\omega t+\theta_k)}+\sum_{l=6n+1}jl\omega LI_{flm}e^{j(l\omega t+\theta_l)} \tag{15}$$
$$=U_{f1m}e^{j(\omega t+\varphi_1)}+\sum_{k=6n-1}U_{fkm}e^{-j(k\omega t+\varphi_k)}+\sum_{l=6n+1}U_{flm}e^{j(l\omega t+\varphi_l)}-U_{sm}e^{j\omega t}$$

Obviously, the real and the imaginary part are equal in both sides respectively, and it is true for any ωt. So equation (15) can be simplified as:

$$\omega LI_{f1m}=U_{f1m}-U_{sm},\varphi_1=0,\theta_1=-\pi/2 \tag{16}$$

$$k\omega LI_{fkm}=U_{fkm},\varphi_k=\theta_k+\pi/2 \tag{17}$$

$$l\omega LI_{flm}=U_{flm},\varphi_l=\theta_l+\pi/2 \tag{18}$$

According to equations (16 - 18), the harmonics of APF output current depends on each harmonic of PWM inverter output voltage and the voltage of the power grid.

Moreover, PWM inverter amplitude modulation ratio M is the ratio of the length of output voltage resultant vector U_{fr} and half of the average DC voltage U_{dc}.

$$M=\frac{2U_r}{U_{dc}} \tag{19}$$

$$U_{fr}=\left\|U_{f1m}e^{j(\omega t+\varphi_1)}+\sum_{k=6n-1}U_{fkm}e^{-j(k\omega t+\varphi_k)}+\sum_{l=6n+1}U_{flm}e^{j(l\omega t+\varphi_l)}\right\| \tag{20}$$

Considering compensating the load in the worst case, the maximum value of U_{fr} can be expressed by equation (21).

$$U_{fr}|_{\max}=U_{f1m}+\sum_{k=6n-1}U_{fkm}+\sum_{l=6n+1}U_{flm} \tag{21}$$
$$=U_{sm}+\omega LI_{f1m}+\sum_{k=6n-1}k\omega LI_{fkm}+\sum_{l=6n+1}l\omega LI_{flm}$$

The maximal U_{fr} is the biggest PWM inverter output voltage necessary to compensate harmonic currents of nonlinear load under the worst condition. As for PWM inverter, an APF must output the voltage vector exceeding the maximum, so as to completely compensate harmonic currents of nonlinear load. Based on the above analysis and combining equations (19) and (21), we can get:

$$\frac{MU_{dc}}{2}-U_{sm}\geq\omega LI_{f1m}+\sum_{k=6n-1}k\omega LI_{fkm}+\sum_{l=6n+1}l\omega LI_{flm} \tag{22}$$

$$U_r\leq\frac{U_{dc}}{\sqrt{3}},M\leq\frac{2}{\sqrt{3}}=1.1547 \tag{23}$$

Equation (23) indicates the linearity range of space vector modulation. Suppose that the amplitude modulation ratio M is constant and equals to or more than 1.1547during the operation of APF, then formula (22) can be transformed to:

$$U_\Delta\geq\omega LI_{f1m}+\sum_{k=6n-1}k\omega LI_{fkm}+\sum_{l=6n+1}l\omega LI_{flm} \tag{24}$$

$$U_\Delta=\frac{U_{dc}}{\sqrt{3}}-U_{sm} \tag{25}$$

From the analysis of the above two equations, it can be concluded that:

(1) U_Δ determines the capacity of APF output harmonic current;

(2) With the same harmonic current RMS, the higher the order of harmonics is, the bigger PWM inverter output

harmonic voltage is required;

(3) The influence on PWM inverter output harmonic voltage caused by the size of output inductor L is a factor to be considered when designing L.

Here to analyse the influence of U_{Δ} on the capability of APF output harmonic current. Assume that the designed output inductor L=0.3mH, the rated grid phase voltage RSM U_{sn}=220V, and the nominal DC voltage U_{dcn}=700V.Based on the above design conditions, the compensation performance of APF can be achieved to meet the requirements. If the grid voltage fluctuates in a range of 90%-110%, the capability of APF output harmonic current varies with the changed U_{Δ}.

As shown in Fig. (**4**), the vertical axis shows the peak of the maximum *k-th* harmonic current that APF can output with the corresponding grid voltage. When U_s =220V, the peak of maximum *5-th* harmonic current is 197.5A, and when U_s=1.1U_{sn}=242V, the peak one is 131.4A, and it is 263.6Awhen U_s=0.9U_{sn}=198V. Comparing the grid voltage 1.1U_{sn} with U_{sn}, the capacity of APF output the maximum *5-th* harmonic current declines by almost 33.5%. There is a similar relationship for other harmonics.

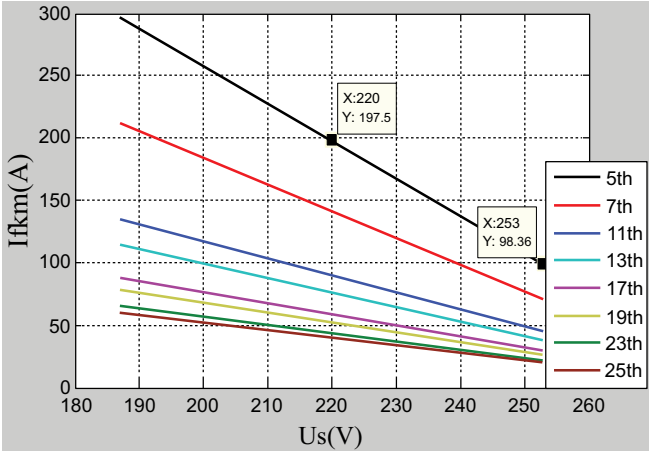

Fig. (4). The capability of APF output harmonics when the grid voltage varies.

In conclusion, without considering the impact of current regulator and the error of harmonic extraction process, U_{Δ} will influence on the compensation performance of APF. In the linear modulation range and with the constant modulation ratio, increasing DC voltage can enhance the compensation performance of APF, while decreasing DC voltage can reduce the performance. Similarly, any increase/decrease in the grid voltage leads to a relative decrease/increase on the APF compensating performance.

5. OPTIMIZING DC VOLTAGE CONTROL BY ADOPTING THE DROOP REGULATOR

5.1. Design of the Droop Regulator

In industrial fields, the line voltage generally has no sudden changes, while it tends to be on large fluctuation (range:90%-110%) over a long period of time. The designed DC voltage is bigger in the worst case of grid voltage when taking U_s = 1.1U_{sn}. A larger DC voltage can cause more power loss according to the analysis above. However, if the grid nominal voltage is used in the design of the DC voltage, it is likely that the compensation performance of APF cannot be ensured with the increase of the grid voltage.

Assuming that at rated grid voltage, the compensation performance of APF can meet the expected requirement by using the designed DC voltage rating. A droop regulator can be designed to control DC voltage reference with the grid voltage fluctuating according to equation (25). Increasing DC voltage can enhance the compensation performance of APF with a higher grid voltage, while decreasing DC voltage can reduce the power loss of APF with a lower grid voltage. Thus, the integrative optimization of APF's power loss and compensation performance is implemented.

The droop regulator can be expressed by the following equations (26) and (27):

$$U_{\Delta n} = \frac{U_{dcn}}{\sqrt{3}} - \sqrt{2}U_{sn} = 93V \quad (26)$$

$$U_{dc\_ref} = \sqrt{3}\left(U_{\Delta n} + U_{sm}\right) \quad (27)$$

On the basis of the grid voltage fluctuating in the range of ±10% (APF is no longer working if the grid voltage is out of this range), the droop regulator curve can be drowned according to the above two equations. As shown in Fig. (**5**), the range of DC voltage is 646V-754V.

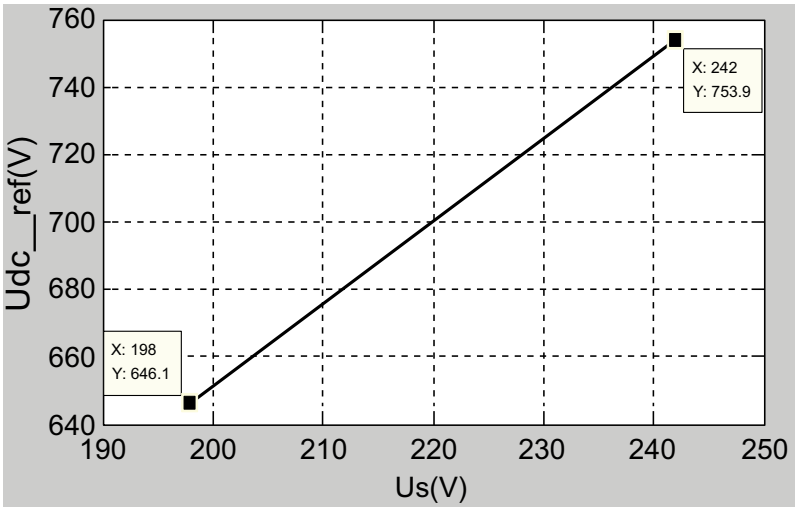

Fig. (5). Controlling DC voltage by the droop regulator.

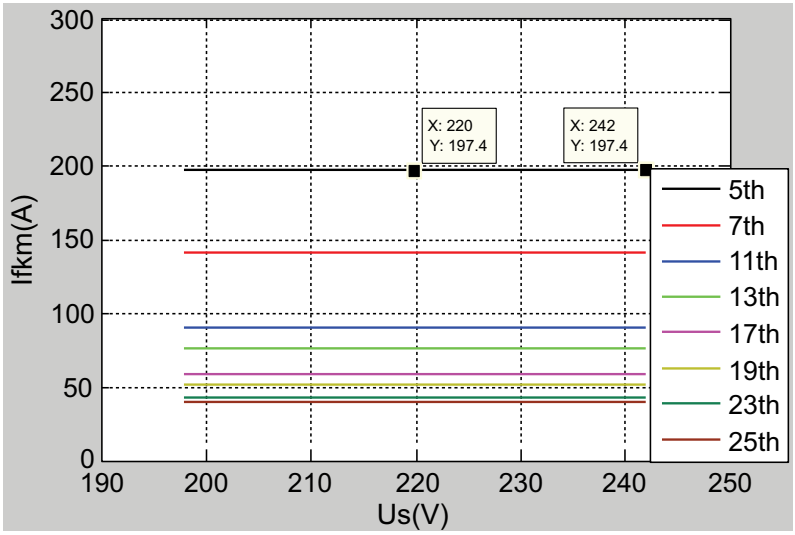

Fig. (6). The capability of APF output harmonics current when the grid voltage varies by using the droop regulator.

Further, the influence on the capacity of APF output harmonic current caused by the grid voltage fluctuating after using the droop regulator is analysed. It is observed from Fig. (**6**) that the grid voltage fluctuating does not affect the capability of APF output harmonic current in comparison with no droop regulator.

The control strategy of APF by using the droop regulator is shown in Fig. (**7**).

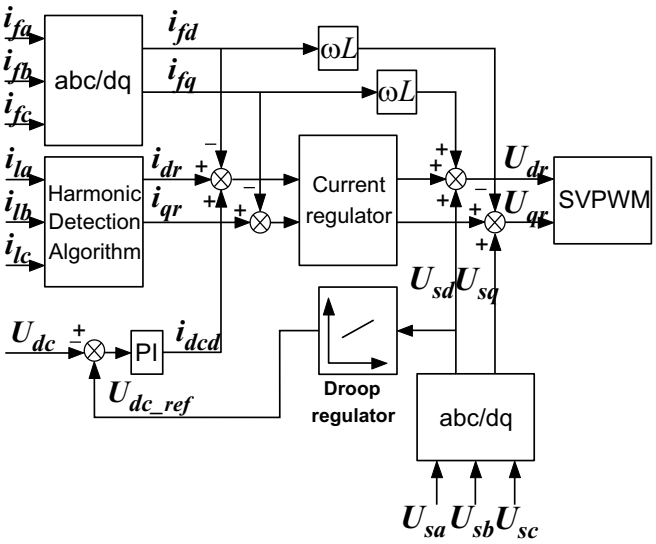

Fig. (7). The control strategy of APF by using the droop regulator.

5.2. Simulation Analysis

This section analyses the relationship among DC voltage`the grid voltage and the compensation performance through MATLAB-SIMULINK simulations. The harmonic source is the three-phase uncontrolled rectifier with resistive load, the RMS of power voltage rating is 380V, and DC voltage rating is 700V. The above analysis is verified under three working conditions.

In Fig. (**8**), the grid voltage remains invariable, and the DC voltage reference is 646V in 0-0.4s, or 700V in 0.4-0.8s, or 754V in 0.8-1.2s.

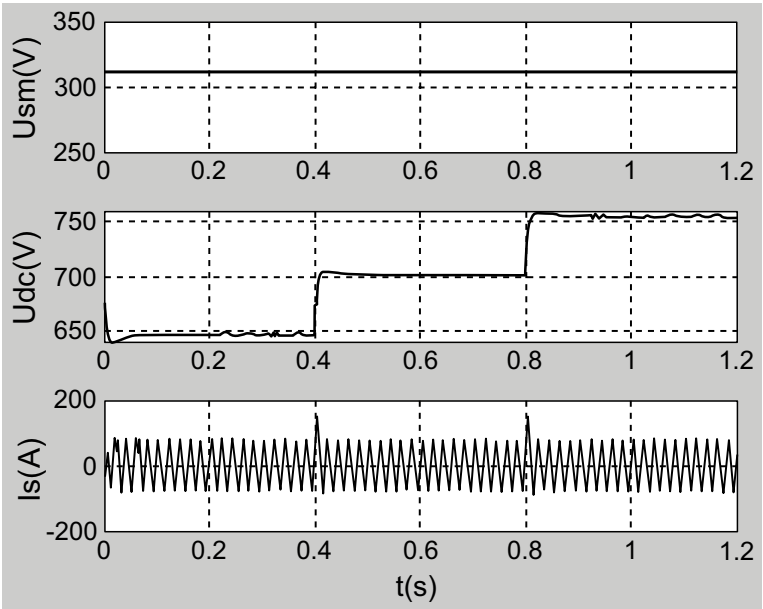

Fig. (8). Waveforms of the grid phase voltage peak U_{sm}`DC voltage U_{dc} and the compensated source current I_s in the first working condition.

It can be seen from Fig. (**9**) that when maintaining the DC voltage constant, the grid voltage is 90% of the rating in 0-0.4s, 100% in 0.4-0.8s, and 110% in 0.8-1.2s.

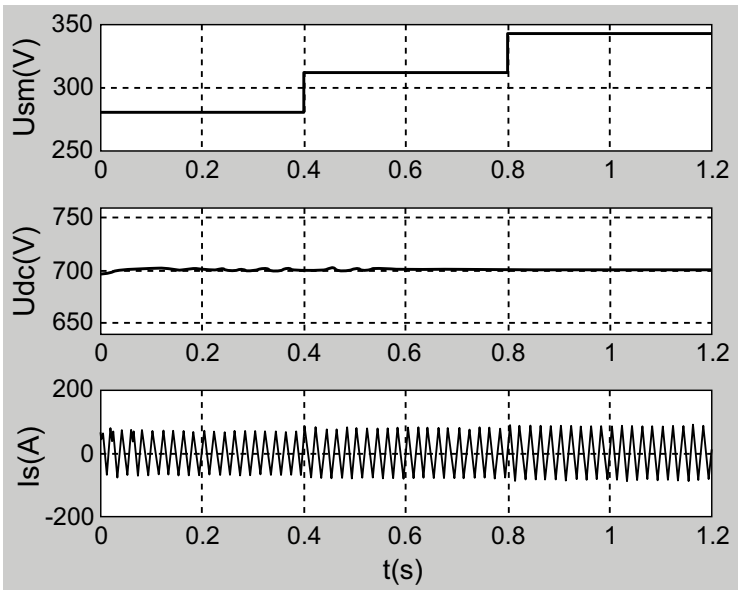

Fig. (9). Waveforms of the grid phase voltage peak U_{sm}`DC voltage U_{dc} and the compensated source current I_s in the second working condition.

As seen from Fig. (**10**), in case of using the droop regulator to control DC voltage, the grid voltage is 90% of the rating in 0-0.4s,100% in 0.4-0.8s, and110% in 0.8-1.2s.

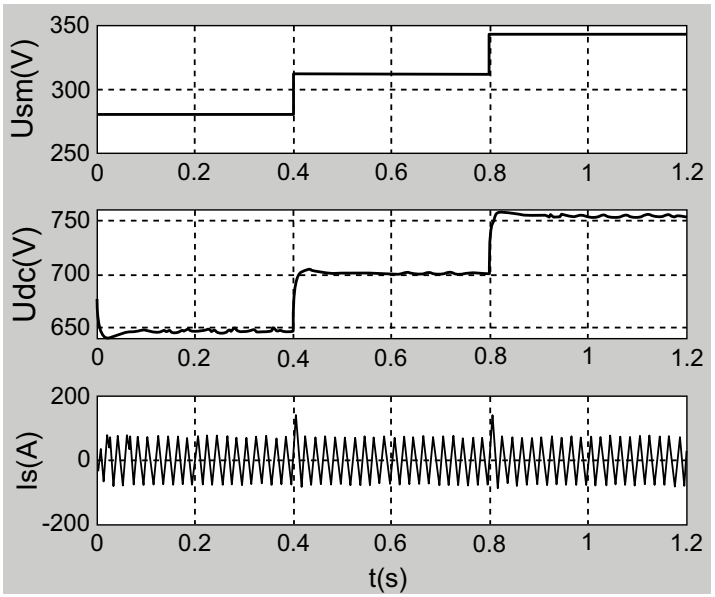

Fig. (10). Waveforms of the grid phase voltage peak U_{sm}`DC voltage U_{dc} and the compensated source current I_s in the third working condition.

According to the simulation results, the performance of APF system in different conditions is analysed as listed in Table **1**. U_s% means the ratio of the real value to the rating of the grid voltage, I_l means the RMS of load current, and *THDI* is the total harmonic distortion of current.

Table 1. The performance of APF system in three working conditions.

Working conditions	U_s%	U_{dc}/(V)	I_l/(A)	*THDI* /%
I	100%	646	70.88	3.12
	100%	700	70.88	2.78
	100%	754	70.88	2.43

(Table 1) contd.....

Working conditions	U_s%	U_{dc}/(V)	I_l/(A)	*THDI* /%
II	90%	700	63.71	2.57
	100%	700	70.88	2.78
	110%	700	78.76	3.01
III	90%	646	63.71	2.80
	100%	700	70.88	2.78
	110%	754	78.76	2.85

For case one, with the constant grid voltage U_s, *THDI* decreases as U_{dc} increases. For case two, with the fixed DC voltage U_{dc}, *THDI* increases as U_s increases. The two simulation conditions both show that the change of U_Δ influences the compensation performance of APF. For case three, compared to case two, the compensation performance of APF can be improved as the grid voltage increases with the help of the droop regulator to control DC voltage.

5.3. Experimental Verification

A series of experiments are employed for the developed APF system to testify the above theoretical analysis. The APF system parameters are given in Table **2**. The nonlinear load is three-phase uncontrolled rectifier with LR connection. The DC-link inductor and the resistor are designed as $0.5mH$ and 5Ω, respectively.

Table 2. The circuit parameters of the APF system.

Parameters	Values	Specifications
U_{sn} (V)	220	The grid phase voltage rating
L(mH)	0.3	The output inductor
C(mF)	10	DC-link capacity
f_c(Hz)	9600	The switching frequency
I_{fm}(A)	100	The maximum output current

Firstly, verify the relationship between compensation performance`power loss and DC voltage. The grid phase voltage maintains 220V, DC voltage reference values are650`700and750Vcorresponding to the first`second and third working condition, respectively and the experiment results are shown in Figs. (**11**-**13**).

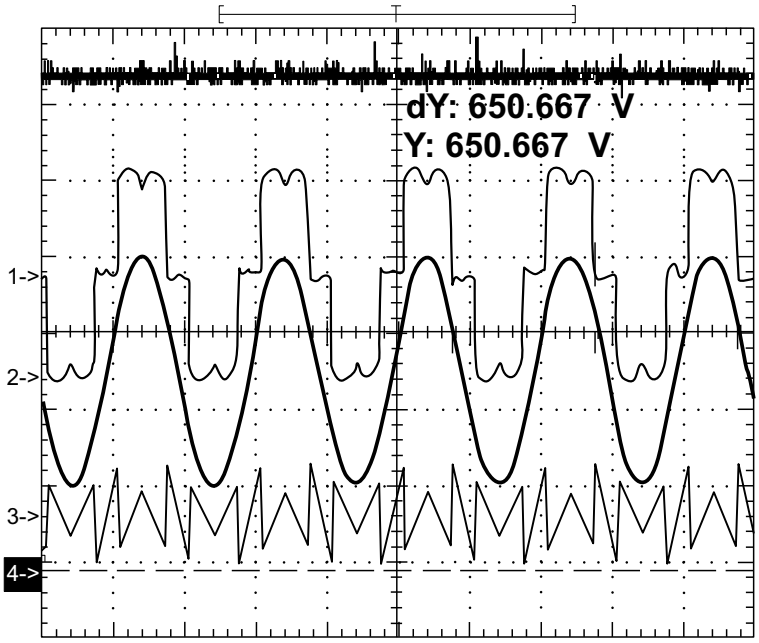

Fig. (11). The first condition, U_s =220V, U_{dc}=650V. The curves 1 ` 2 ` 3 respectively represent A-phase load current`the grid current and APF output current (50A /div), curve 4 is DC voltage (100V/div), 10ms/div.

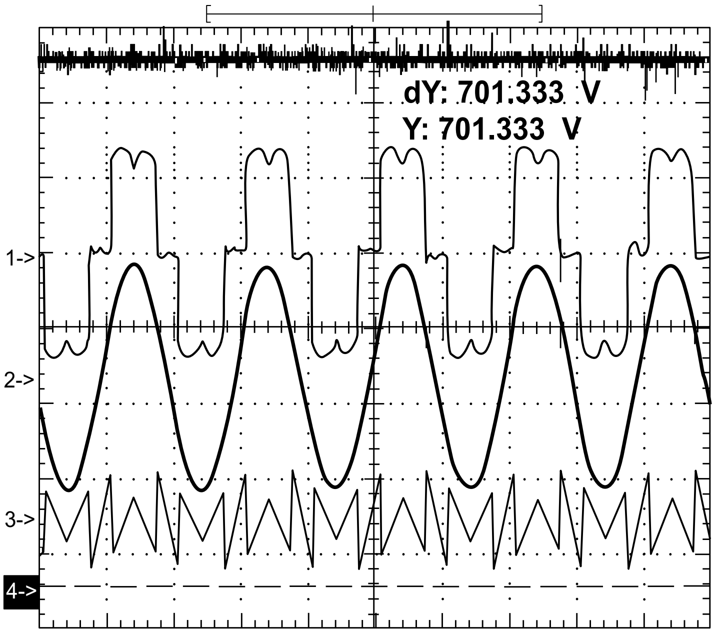

Fig. (12). The second condition, U_s =220V, U_{dc}=700V. The curves 1`2`3 respectively represent A-phase load current`the grid current and APF output current (50A/div), curve 4 is DC voltage (100Vdiv), 10ms/div.

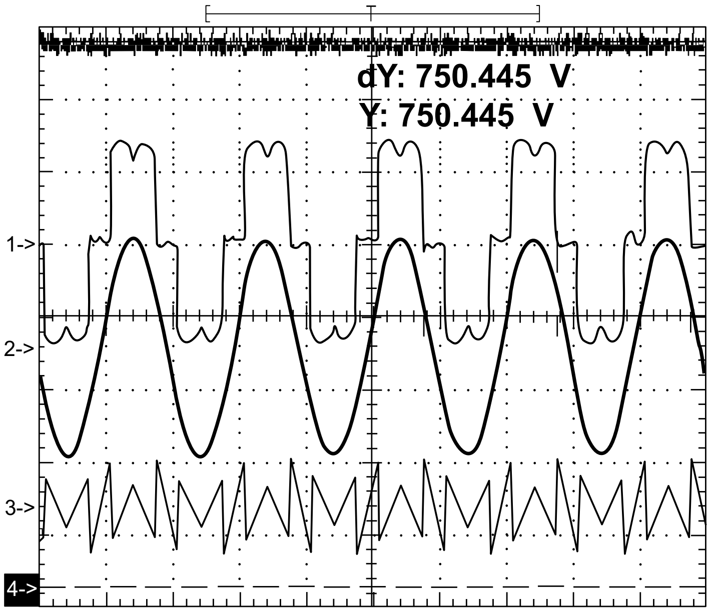

Fig. (13). The third condition, U_s =220V, U_{dc} =750V. The curves 1 , 2 , 3 respectively represent A-phase load current `the grid current and APF output current (50A /div), curve 4 is DC voltage (100V/div), 10ms/div.

Secondly, verify the influence on the compensation performance of APF caused by the grid voltage fluctuating. The DC voltage reference value is700V, and the grid phase voltage is 232V, which is corresponding to the forth condition, shown in Fig. (**14**).

Finally, verify the influence on the compensation performance of APF when adjusting DC voltage with the droop regulator. The grid phase voltage is 232V, and the output DC voltage reference of the droop regulator is 720V, corresponding to the fifth condition, shown in Fig. (**15**).

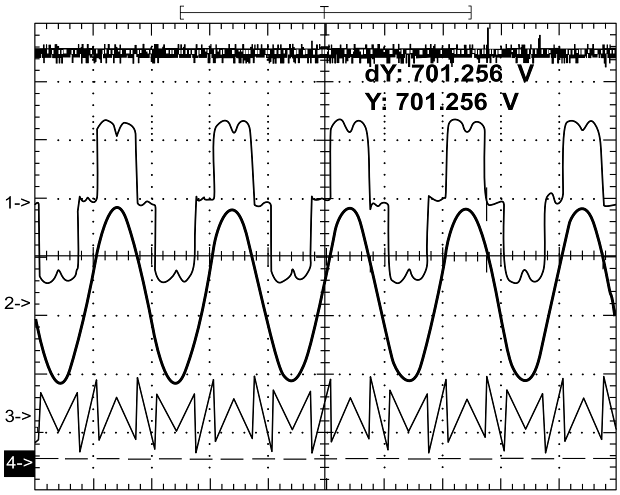

Fig. (14). The forth condition, U_s =232V, U_{dc}=700V. The curves 1 , 2, 3 respectively represent A-phase load current`the grid current and APF output current (50A /div), curve 4 is DC voltage (100V/div), 10ms/div.

According to the experimental results, the performance of APF system in different conditions is analysed as listed in Table **3**. U_s is the grid phase voltage, I_l is the RMS of load current, and *THDI* is the total harmonic distortion of current, P_{loss} is the APF conversion system loss.

Table 3. The performance of APF system in five working conditions.

Working conditions	U_s/(V)	U_{dc}/(V)	I_l/(A)	*THDI* /%	P_{loss}/(KW)
1	220	650	53.44	3.774	3.035
2	220	700	53.46	3.555	3.437
3	220	750	53.47	3.299	3.921
4	232	700	56.51	3.644	3.629
5	232	720	56.55	3.560	3.854

In summary, analysis of case 1`2 and 3, *THDI* decreases and P_{loss} increases during the DC voltage rises if U_s is constant. From case 2 and 4, it can be concluded that if the DC voltage has no change, *THDI* increases with the increased U_s. Compared case 4 with 5, adjusting DC voltage with the droop regulator can improve compensation performance of APF as U_s increases. Finally, comprehensive analysis of these five conditions, it is believed that any decrease in the grid voltage U_s can cause the power loss of APF when adjusting DC voltage with the droop regulator.

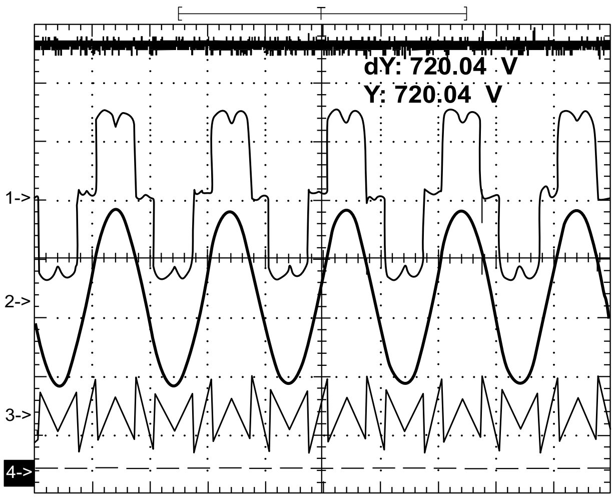

Fig. (15). The fifth condition, U_s =232V, U_{dc}=720V. The curves 1`2`3 respectively represent A-phase load current`the grid current and APF output current (50A /div), curve 4 is DC voltage (100V/div), 10ms/div.

And finally, the dynamic performance of APF is verified when the DC-link voltage is suddenly changed. As shown in Fig. (**16**), when the grid phase voltage maintains 220V, the DC voltage surges from700V to 650V. Besides, the compensated grid current has some fluctuation but little in the overshoot process.

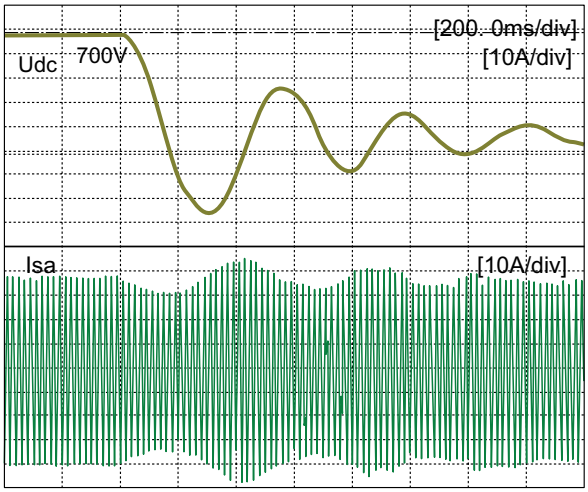

Fig. (16). The dynamic performance of APF when DC voltage is suddenly changed.

CONCLUSION

This paper firstly describes the design of DC voltage regulator in detail, and then the influence on the power loss and compensation performance of APF caused by DC voltage is analysed. According to the analysis`simulations and experiments, some important results have been gotten. Any increase/decrease in DC voltage can cause increase/decrease in the power loss of APF. Besides, without considering the influence of current regulator and the error of harmonic extraction process, the compensation performance of APF increases with the rising of DC voltage, as well as it decreases as the grid voltage rises. A higher DC voltage can improve compensation performance with the increased grid voltage. Also, on the basis of guaranteeing the compensation performance, a lower DC voltage can reduce power loss when the grid voltage decreases. Therefore, a new control strategy for adjusting DC voltage with the droop regulator is proposed. Adjusting DC voltage with the use of droop regulator can keep U_{Δ} constant as the grid voltage fluctuates, and what can be achieved the integrative optimization of APF's power loss and compensation performance.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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