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Optimum Design for Eliminating Back Gate Bias Effect of Silicon-on-insulator Lateral Double Diffused Metal-oxide-semiconductor Field Effect Transistor with Low Doping Buried Layer

C.H. Ho[1], F.T. Chien[2], C.N. Liao[1] and Y.T. Tsai*[,1]

[1]*Department of Electrical Engineering, National Central University, Taiwan, R.O.C.*

[2]*Department of Electronic Engineering, Feng Chia University, Taiwan, R.O.C.*

Abstract: An optimum design with silicon-on-insulator (SOI) device structure was proposed to eliminate back gate bias effect of the lateral double diffused metal-oxide-semiconductor field effect transistor (LDMOSFET) and to improve breakdown voltage. The SOI structure was characterized by low doping buried layer (LDBL) inserted between the silicon layer and the buried oxide layer. The LDBL thickness is a key parameter to affect the strong inversion condition in the back MOS capacitor of the new SOI diode. The optimum design of LDBL thickness for the SOI diode was 2.65 μm. Furthermore, the breakdown capability has been improved 11%.

INTRODUCTION

Dielectric isolation is a reliable technique for high voltage power IC's. High voltage lateral devices fabricated on silicon on insulator (SOI) wafer due to its superior isolation with low leakage current, and silicon dioxide can endure higher voltage than silicon [1, 2]. In the design of lateral SOI power device, one of the key points is the reduction of electric field along the semiconductor surface of the drift region [3]. Since the area efficiency of the device is determined by its drift region length, minimization of the drift region length for a device with a given breakdown voltage is desirable and has received attention recently in two-dimensional (2-D) simulations [4] as well as in an experimental investigation [5]. The performance of SOI device is affected by the substrate bias. For a power diode built by SOI technology, the influence of the substrate bias on the breakdown voltage is eliminated by inserting a semi-insulating polycrystalline silicon layer (SIPOS) [6]. But the SIPOS layer is not compatiable with the standard power IC technology, because the leakage current is increased by the SIPOS over silicon interface traps [7, 8].

However, no analysis of device physic has been so far given for the substrate bias effect on SOI device breakdown voltage. In this paper, the analysis of the substrate bias effect for the lateral and vertical surface potential and electric field distribution in the off-state is firstly proposed, and a novel SOI device structure with a low doping buried layer (LDBL) is employed to eliminate the substrate bias effect. The 2-D simulations for the substrate effect are performed using the tool ISE-TCAD [9].

BACK GATE BIAS EFFECT IN THE SOI DEVICE

Fig. (**1**) shows the device structure which has 2 μm p- and n-type diffusion layers with a 1×10^{18} cm^{-3} surface impurity concentration. The diffusion layer is formed on a 5 μm thin silicon layer over a 0.8 μm silicon dioxide substrate. The buried oxide can be treated as an n-type substrate metal-oxide-semiconductor (MOS) capacitor as shown in Fig. (**1**). The substrate bias voltage (V_{sb}) is the designated as the back gate bias voltage. Therefore, as shown in Fig. (**2**), the operation of the V_{sb} includes (1) accumulation region, (2) depletion region, and (3) strong inversion region. Firstly, the breakdown voltage is increased lightly as the positive V_{sb} increases, but it is decreased as soon as the positive V_{sb} increases at the accumulation region. Secondly, the breakdown voltage is decreased as the negative V_{sb} increases at the depletion region.

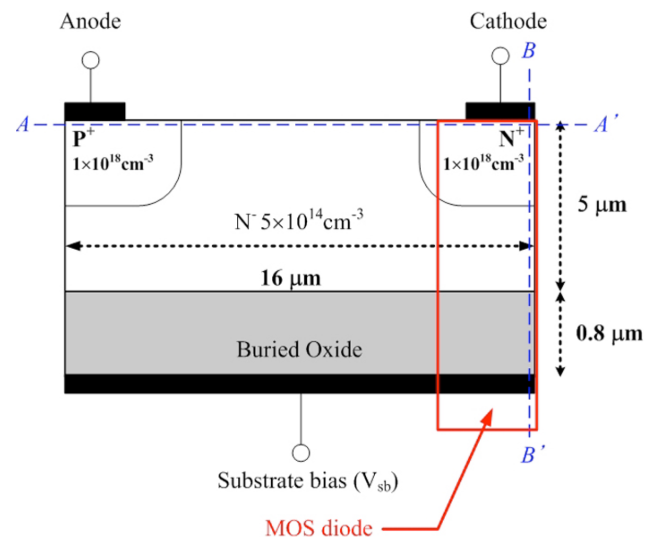

Fig. (1). Cross-section of the conventional SOI diode structure.

Finally, the breakdown voltage is kept even if the negative V_{sb} increases at the strong inversion region. In order to analyze the potential and the electric field inside the SOI diode, the cathode of device should be fixed at the same bias

*Address correspondence to this author at the Department of Electrical Engineering, National Central University, R.O.C., Taiwan; Tel: 886-3-4227151 ext. 34450; Fax: 886-3-4255830;
E-mail: yttsai@ncu.edu.tw

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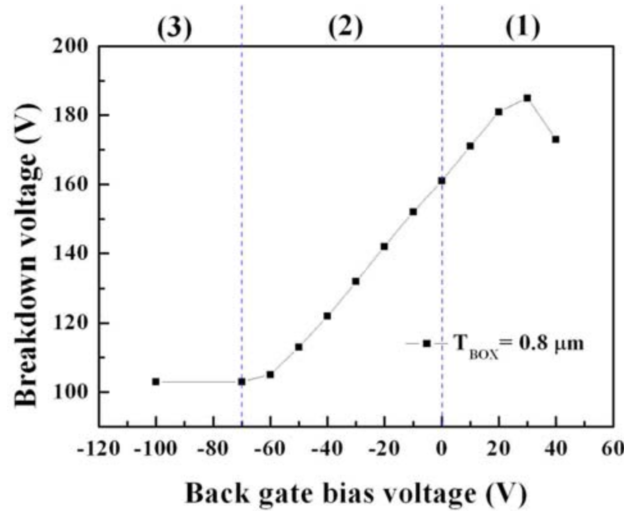


Fig. (2). Influence of the V_{sb} on breakdown voltage.

condition. Therefore, the cathode is biased at 100 V before breakdown, and the V_{sb} is biased at 40 V, 30 V, 20 V, 10 V, 0 V, -30 V, -60 V, -70 V and -100 V with the same device structure, respectively. The breakdown voltage was affected by the V_{sb} in the SOI diode as explained later.

Notice that, to save computation time, the SOI simulated structure does not include the underlying mechanical silicon. This was replaced by a silicon electrode directly placed under the back gate, without loosing direct-current (DC) simulations validity and accuracy.

ACCUMULATIOM REGION

The breakdown voltage is increased lightly as the positive V_{sb} increases, but it is decreased as soon as the positive V_{sb} increases as shown in region 1 of Fig. (**2**). When the back gate terminal is biased with positive voltage, the back MOS acts as accumulation mode MOS capacitor with an n-type substrate. The electrons are attracted toward the buried oxide surface.

Fig. (**3**) shows equi-potential lines were more concentrated near the anode was observed at point 1 as the V_{sb} increases, and were more dispersed at the MOS diode portion was observed at point 2, as shown in Fig. (**1**), as the V_{sb} increases. The MOS diode portion consists of n^+-cathode, n^- layer, buried oxide and the substrate [7]. Therefore, the cath-

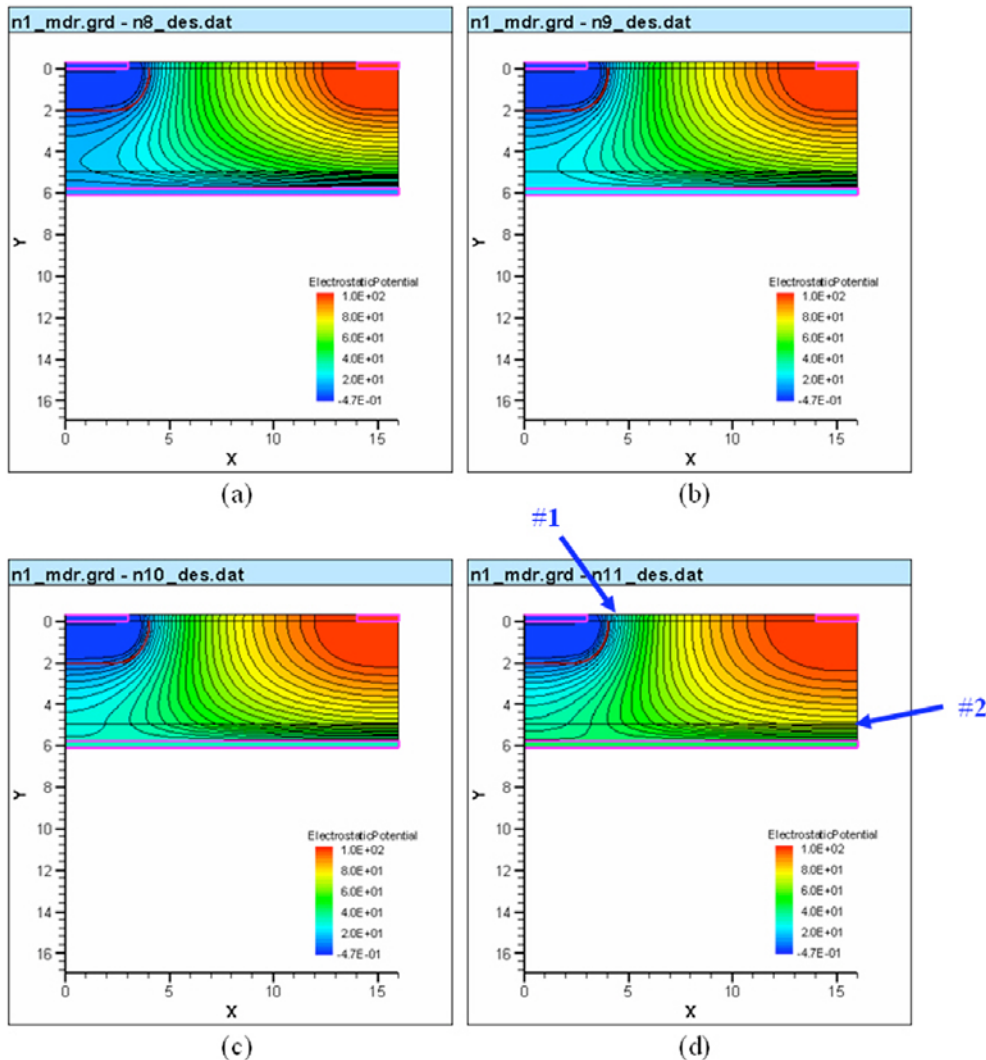


Fig. (3). Potential distribution of the positive V_{sb}. Equi-potential lines are 3.3 V/line. (**a**) V_{sb}= 10 V, (**b**) V_{sb}= 20 V, (**c**) V_{sb}= 30 V, and (**d**) V_{sb}= 40 V.

ode voltage drops on the p-n junction near the anode terminal.

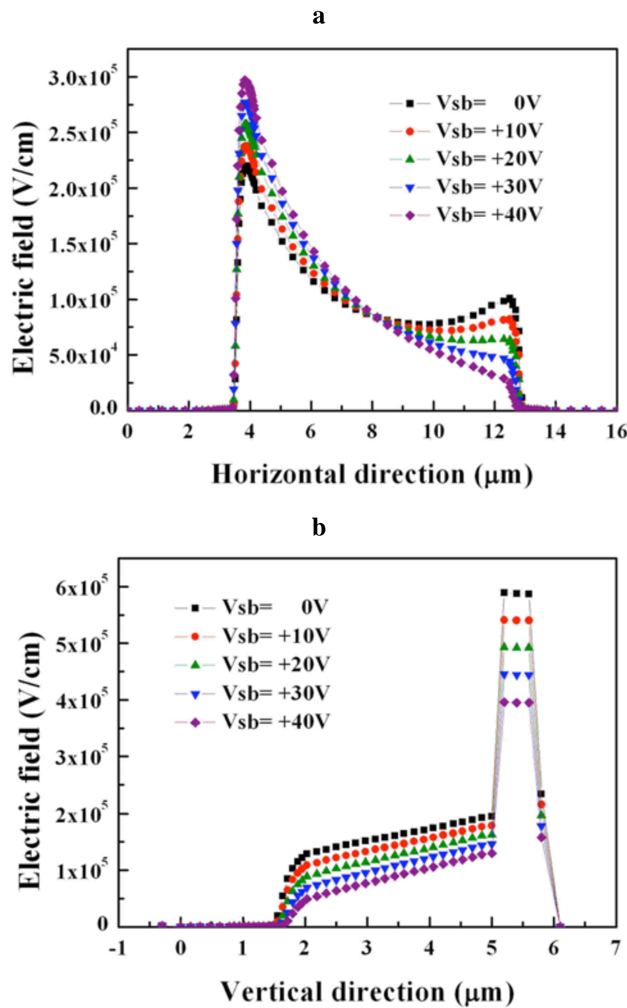


Fig. (4). Electric field distribution along the axis (**a**) *A-A'* and (**b**) *B-B'*. A high electric field is successfully applied at the p^+-n junction as the V_{sb} bias increases.

Fig. (**4**) shows the electric field distribution along the axis *A-A'* and *B-B'* of the calculated device for positive bias of V_{sb}. The electric field of the p-n junction rises as the positive V_{sb} increases, as shown in Fig. (**4a**), and the electric field of vertical direction reduces as the positive V_{sb} increases as shown in Fig. (**4b**). Breakdown is dominated by the p-n junction curvature effect [10] at this region.

DEPLETION REGION

The breakdown voltage is decreased as the negative V_{sb} increases as shown in region 2 of Fig. (**2**). When the V_{sb} terminal is biased with negative voltage from 0 V to -60 V, the back MOS acts as the depletion mode MOS capacitor with an n-type substrate as shown in Fig. (**5**).

The electrons are depleted toward the surface direction, and the depletion region extends along the buried oxide surface. The electric field of the horizontal direction does not change as the negative V_{sb} increases from -30 V to -100 V as shown in Fig. (**6a**), but the electric field of the vertical direction rises as the negative V_{sb} increases as shown in Fig. (**6b**). Furthermore, the electric field of the horizontal direction is smaller than the maximum critical silicon electric field of 2.5×10^5 V/cm [11]. Therefore, breakdown is dominated by the MOS diode portion at this region. The reason for this is that the whole potential drop has to be supported vertically along *B-B'*. The phenomena will be understood from Fig. (**6b**). A high electric field inside the buried oxide layer induced a high electric field inside the silicon layer near the interface and limited the breakdown voltage.

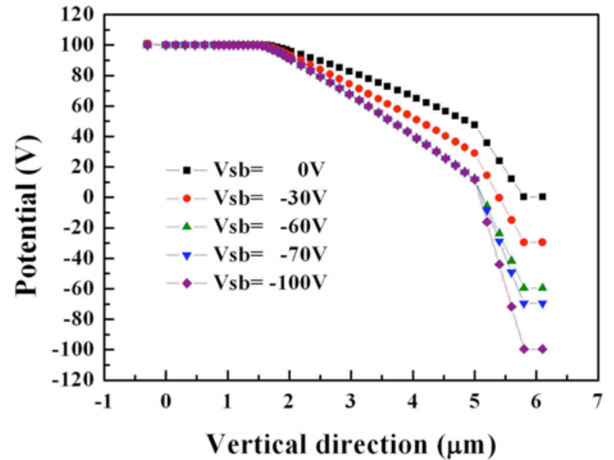


Fig. (5). Potential distribution along the axis *B-B'* at the negative V_{sb}.

STRONG INVERSION REGION

When the back gate terminal is biased with large negative voltage from -70 V to -100 V, the back gate MOS capacitor reaches to the strong inversion region as shown in Fig. (**5**). The breakdown voltage does not decrease until the negative substrate bias reaching to the -70 V, and it is kept at 108 V as shown in region 3 of Fig. (**2**). It can be attributed to that the negative substrate bias reaches the strong inversion of the back MOS capacitor. The space charge width has reached its maximum value. The interface between n^- layer and the buried oxide has been inverted from electron to hole, and the holes inversion layer charge was created. Therefore, the voltage drops only on the buried oxide, and it is seen that the electric field is effectively shielded inside the buried oxide layer as shown in Fig. (**6b**). Hence, breakdown is dominated by the MOS diode portion at this region. At the same time, the electric field is kept in the silicon layer.

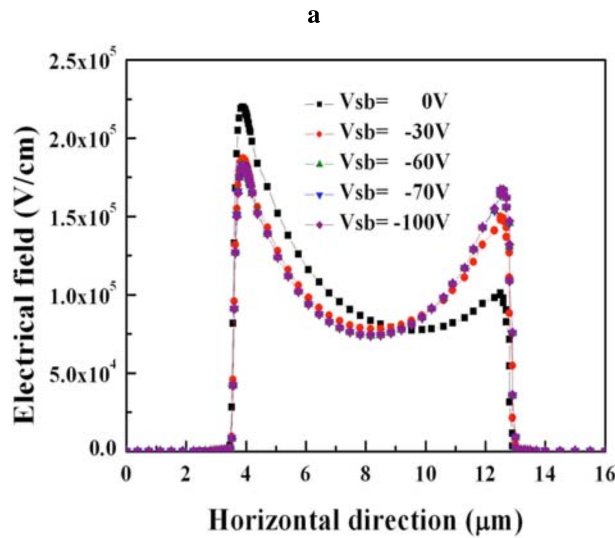
SIMULATION RESULTS AND DISCUSSION

Optimum Design for Eliminating Back Gate Effect

Fig. (**7**) shows the cross section of the proposed novel SOI sturcture. The novel SOI sturcture is characterized by a 1.5×10^{10} cm^{-3} low doping buried layer (LDBL) inserted between the silicon layer and the buried oxide layer. All of the device parameters are the same with the conventional structure except for the LDBL as shown in Fig. (**1**).

The LDBL can effectively shield the influence of the substrate bias. Therefore, the novel SOI structure has higher breakdown voltage than the conventional SOI structure. Fig. (**8**) shows that the LDBL thickness is a key parameter to affect the strong inversion condition in the back MOS

a



b

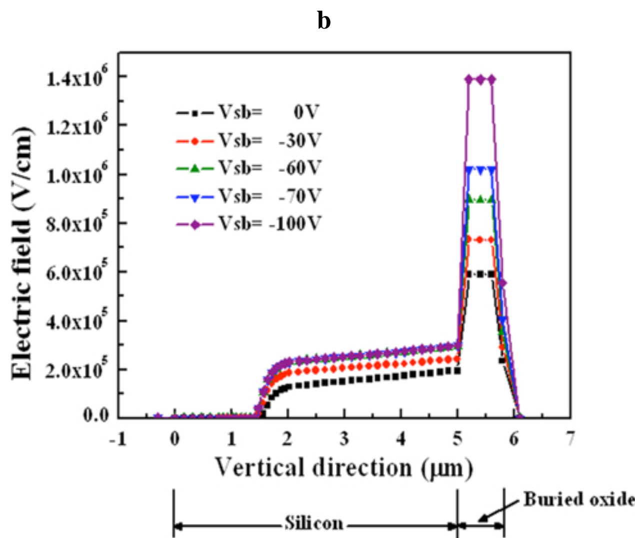


Fig. (6). Electric field distribution of the conventional structure along the axis (**a**) *A-A'* and (**b**) *B-B'*.

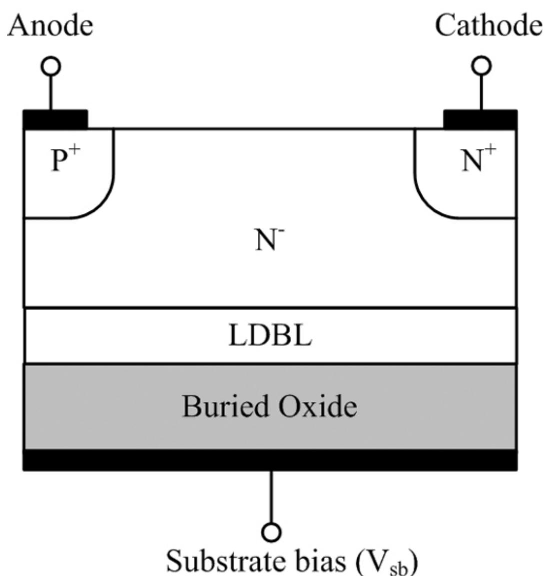


Fig. (7). Cross-section of the novel SOI diode structure.

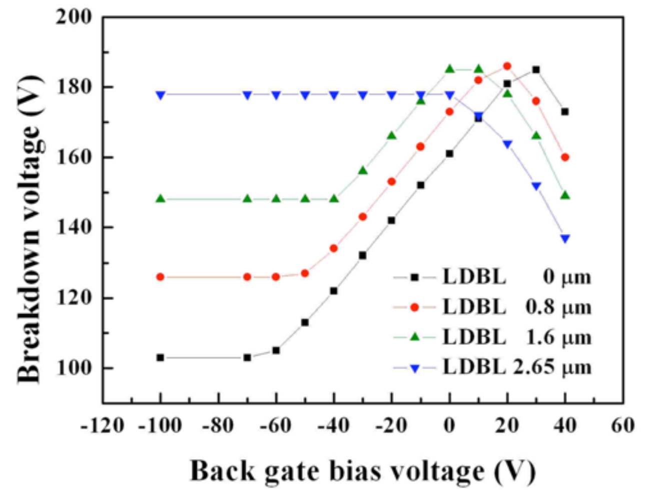
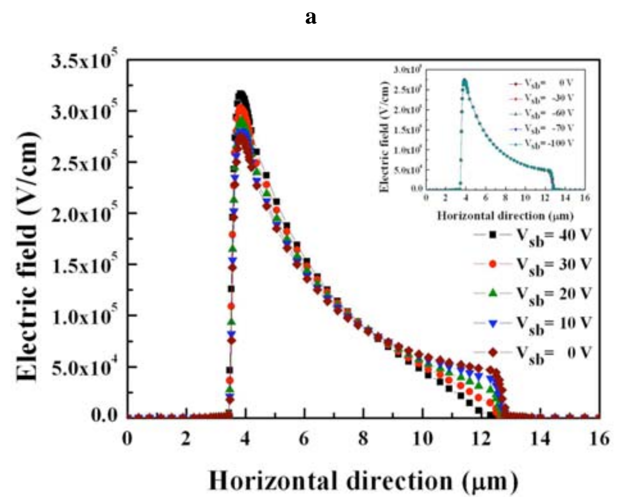


Fig. (8). Effects of back gate bias voltage on breakdown voltage in the SOI diode.

a



b

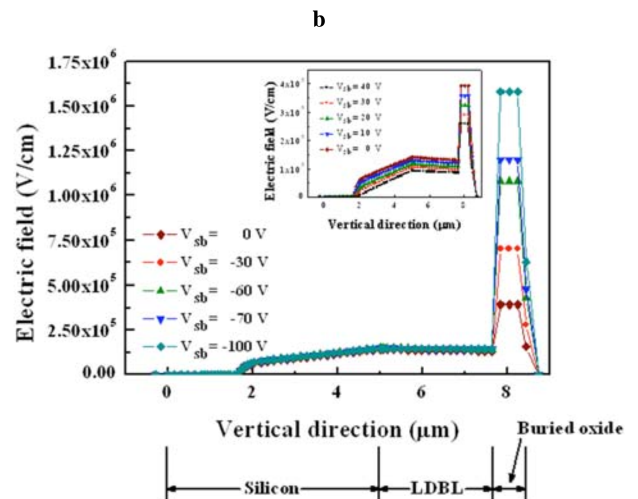


Fig. (9). Electric field distribution of the novel structure at LDBL= 2.65 μm along the axis (**a**) *A-A'* and (**b**) *B-B'*.

capacitor of the novel SOI diode. The cathode is biased at 100 V before breakdown, and the V_{sb} is biased at 40 V, 30 V, 20 V, 10 V, 0 V, -30 V, -60 V, -70 V and -100 V with each device structure, respectively. In the conventional structure

where LDBL thickness equal to 0 µm, the diode breakdown voltage decreases as the negative V_{sb} increases. As we expected, it was confirmed that the diode breakdown voltage was not affected by the negative V_{sb} as the LDBL thickness increases. For the case of $V_{sb} \leq 0$ V, the optimum structure appears at LDBL = 2.65 µm. On the other hand, the strong inversion codition of the novel SOI diode happen earily compared to the conventional one, and the absolute of substrate bias for reaching to the strong inversion condition is smaller as the LDBL thickness increases as shown in Fig. (**8**). Fig. (**9**) shows the electric field distribution along the axis *A-A'* and *B-B'* of the novel structure when the thickness of LDBL is 2.65 µm.

The electric field of the p-n junction rises as the positive V_{sb} increases, but it is kept as the negative V_{sb} increases as shown in Fig. (**9a**). Furthermore, the vertical electric field of the MOS diode portion seems to be shielded inside the buried oxide layer as shown in Fig. (**9b**). Comparison between horizontal and vertical electric field, it could be clearly understood that the electric field of the p-n junction is larger than the electric field of the MOS diode region inside the silicon layer. Therefore, breakdown is dominated by the p-n junction curvature effect with the optimum structure.

APPLICATION OF LDMOSFET WITH LDBL

Fig. (**10**) shows the cross-sectional view for the proposed structure of the SOI LDMOSFET with LDBL used in the simulation. The concentration of the n^- epitaxial layer, n^+ source, n^+ drain, and p-body are 5×10^{14} cm^{-3}, 1×10^{18} cm^{-3}, 1×10^{18} cm^{-3}, and 5×10^{16} cm^{-3}, respectively. Fig. (**11**) shows the influence of the breakdown characteristics of the conventional SOI LDMOSFET and the novel SOI LDMOSFET with LDBL. As was expected, it was confirmed that the back gate effect was eliminated at the novel SOI LDMOSFET, and the breakdown capability was improved 11% by inserting the LDBL.

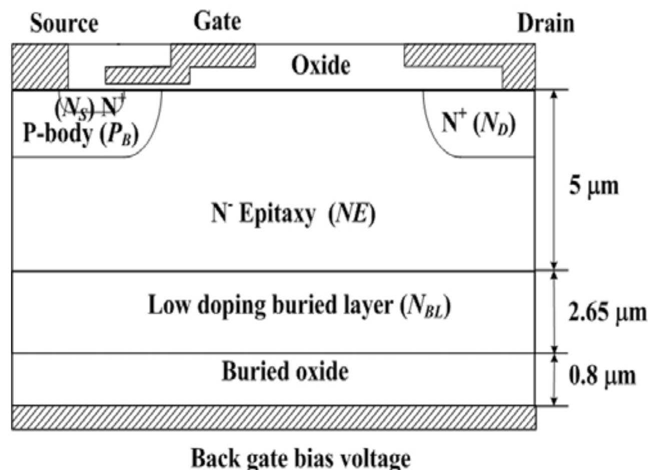


Fig. (10). Cross-section of the SOI LDMOSFET structure with LDBL.

CONCLUSIONS

An optimum design for eliminating back gate bias effect of the SOI device characterized by a LDBL shielding layer inserted between the silicon layer and the buried oxide is predicted by ISE-TCAD simulation tools. The optimum structure appears at LDBL=2.65 µm. Comparison of the simulated results between conventional and novel structures have shown a breakdown voltage improvement. The simple analysis presented in this paper will be useful for design the SOI power devices such as LDMOSFET and lateral insulated gate bipolar transistor (LIGBT) employed with LDBL.

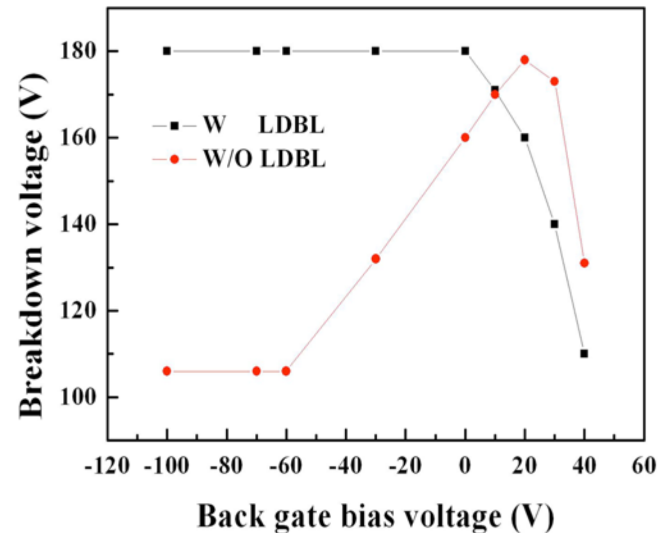


Fig. (11). Effect of back gate bias voltage on breakdown voltage in the SOI LDMOSFET with and without LDBL.

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