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Structural Stress Analysis of 32×32 InSb Infrared Focal Plane Array with Underfill

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Abstract: Based on viscoplastic Anand's model, the structural stress of 8×8 InSb infrared focal plane array detector with underfill is systematically analyzed by finite element method, and the impacts of design parameters including indium bump diameters, heights on both Von Mises stress and its distribution are discussed in this manuscript. Simulation results show that for the given indium bump height, the maximum stress existing in InSb chip is almost unchanged with reduced indium bump diameters, and with thicker indium bump, the stress is smaller, when the indium bump height is over than 15μm, the stress reduces slowly with decreased standing off height. When the InSb IRFPA format increases from 8×8 to 32×32, the maximal Von Mises stress increases from 500MPa to 900Mpa, almost twice over, and is not proportional to array format scale.

Keywords: Finite element method, focal plane array, InSb, structural stress.

1. INTRODUCTION

Indium antimonide (InSb) pn junctions are widely used as infrared photovoltaic detectors and imaging sensors for the 3-5μm spectral range [1, 2]. Photovoltaic diodes are usually placed in rectangular array or square array, then *via* indium bumps, assembled to a silicon readout integrated circuits (ROIC), after that, underfill is dispensed between InSb die and Si ROIC substrate for increasing the reliability of flip-chip packaging. To achieve the lowest level of electronic noise to approach the photon noise limit, it is necessary to cryogenically cool the infrared focal plane array (IRFPA) to liquid nitrogen temperature (77K). Therefore, fracture in InSb chip usually occurs with the rapid temperature dropping process, due to the mismatch in the coefficients of thermal expansion between the silicon multiplexer and the InSb detector array, which will cause mechanical stress/strain on both indium bumps and InSb chip with thickness less than one diffusion length about 8μm. In order to reduce the InSb chip fracture possibility and improve the yield, it is necessary to analyze the induced thermal strain and stress values and its distribution in InSb chip. At present time, the thermo-mechanical reliability of flip-chip assemblies is usually assessed by finite element simulations in conjunction with experimental verification, that is, based on the strain and stress analysis, the structure reliability is assessed [3, 4].

In 2009, Rui Wu Chang research group delivers the constitutive relations of indium in extreme-temperature in Anand's model [5], a rate and temperature dependent constitutive model, applied to represent the inelastic deformation behavior of indium at low temperatures down to -150◦C. Based on the above research results, the structural stress of 8×8 InSb array detector with underfill dependent on both indium bump diameters and thickness is systematically researched by finite element method, for finding the optimal structural sizes to avoid thermal stress concentration in InSb chip.

2. MODEL CREATION AND PARAMETERS SELECTION

When creating the finite element analysis model of InSb IRFPA detector, indium bumps are assumed to be octagonal prisms, and no defects exist in the whole device. InSb IR-PFA is composed of InSb photodiode arrays, indium bumps array, Si ROIC and underfill encapsulant materials, just as shown in Fig. (**1**). InSb chip dimensions are 1600μm×1600μm×8μm, and attached to Si ROIC substrate with 32×32 indium bumps array, Si ROIC substrate dimensions are 1700μm×1700μm×300μm, indium bumps height has been fixed at 24μm with 50μm pitch, and its diameter increases from 20μm to 36μm in step of 4μm. In order to describe the mesa structure locating between neighboring detectors elements, a triangular prism, whose cross section area sides length are 5.66μm, 5.66μm and 8μm, respectively, are employed. Using the geometrical symmetry, only one eighth of the overall package is modeled.

InSb chip and Si ROIC substrate are both considered to be linear elastic materials. All the employed parameters are listed in Table **1**, where E is the Young's modulus, μ is the Poisson's ratio, and CTE is the coefficient of thermal expansion (CTE). Flip chip process is completed at 370K, after that, the selected underfill is dispensed between InSb chip and Si ROIC substrate, the glass transition temperature of underfill is 408K, and the curing process is also operated at

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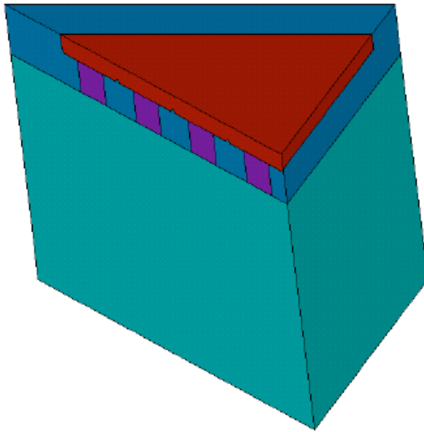

Fig. (1). Three dimensional model of infrared focal plane array device.

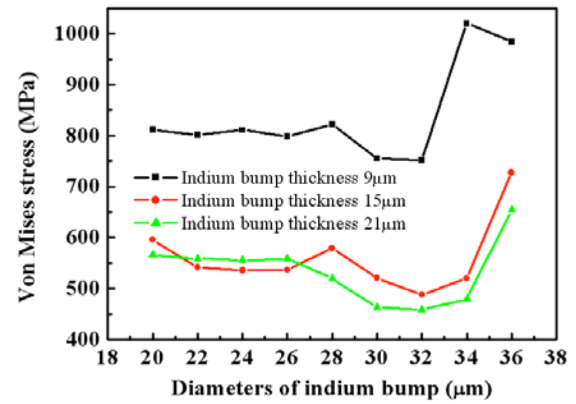

Fig. (2). Von Mises stress maximum values of 8×8 InSb as a function of vaired indium bump diameter with different indium bump heights.

Table 1. Linear Elastic Material Parameters

Materials	Elastic Modulus [E/MPa]	Poison's Ratio [μ]	CTE [α_l ppm/K]
Si ROIC	163000	0.28	2.50
InSb chip	409000	0.35	5.04
Indium bump	10600	0.45	33.00
Underfill	9000	0.3	26.00

408K, at this temperature, no residual stress is assumed to exist within the package. In the simulation, the temperature is gradually reduced from 408K to 77K, which causes thermal stresses to develop. During the temperature drop, no transient heat transfer is considered and the temperature within the model is assumed to be uniform. After about 71 seconds, increments are taken to lower the temperature to ensure the accuracy. Horizontal displacements normal to the symmetrical surfaces are set to zero, at the same time, the displacement of Si ROIC substrate bottom surface center point remains zero.

Indium bump deformation is strongly temperature and time dependent, and associated with the irreversible, temperature and rate dependent inelastic characteristics, which are known to be viscoplastic [6-8]. Here Anand's viscoplastic constitutive model has been used to describe mechanics of constitutive relationship of indium bump [9, 10].

Underfill is an epoxy-based polymer exhibiting time-and-temperature dependent viscoelastic properties. The viscoelastic behavior of underfill can be analyzed using the time-temperature superposition principle, which is based on the empirical observation that the viscoelastic behavior of polymer materials at a reference temperature T_0 can be related to the behavior at another temperature T by changing the experimental time or frequency scale [11-13]. Generally speaking, from the polymers with the glass transition temperature T_0, the shift factor $\log\alpha_T$ was found to be approximately the Arrhenius equation

$$\log\alpha_T = A + \frac{B}{C_2 + T_{ABS}} \quad (1)$$

where A and B are constants, T_{ABS} is the absolute temperature in degrees Kelvin. Using the time-temperature superposition experimental results, it is possible to construct a master curve at an arbitrary reference temperature which extends the relaxation modulus beyond the range of laboratory scale in either the time or the frequency domain. Here the glass transition temperature of underfill T_g is selected as the reference temperature, A Prony series was used to fit the master relaxation curve and this series is of the form

$$G(t) = G_\infty + \sum_{i=1}^{n_G} G_i e^{-\frac{t}{\tau_i}} \quad (2)$$

Where G_∞ represents the equilibrium modulus after the under fill is fully relaxed; G_i and τ_i are the Prony efficient and relaxation time for each element, respectively. The Prony coefficients for the master curve are given in Table **2** [14, 15].

3. SIMULATION RESULTS ANALYSIS

Two-step method is used to research stress and its distribution in 32×32 InSb IRFPA employing finite element method for time saving. First, a small 8×8 InSb IRFPA is systematically studied by varying indium bump diameters, standoff heights in suitable range, simulation results show that as the diameters of indium bump decrease from 32μm to 20μm in step of 2μm, the maximum stress existing in InSb chip increases slowly from 751MPa to 812MPa with 9μm indium bump height, and for thicker indium bump, such as 15μm and 21μm, the maximal Von Mises stress in the InSb chip versus indium bump diameters almost have the same vary tendency, just like the curve is shifted down some values. When the height of indium bump increases from 9μm to 21μm in step of 6μm, the maximal stress in InSb chip first reduces sharply from 800MPa to 500MPa, then almost retains constant, just as shown in Fig. (**2**). Here the temperature of InSb IRFPA is gradually reduced from 370K to 77K in 71 seconds, and the underfill is assumed to be linear elastic properties. Apparently, with thicker indium bump height, the maximal Von Mises stress in InSb chip is lower. To learn the effect from indium bump diameters on the maximal Von Mises stress in InSb chip, and taking manufacturing precision into consideration, here the indium bump height is selected as 24μm for smaller stress.

Table 2. Relaxation Parameters of Viscoelectic Maxwell Model for Underfill

i	C_i	T_i
1	0.0031	2.1230×10^{-10}
2	0.0299	4.5738×10^{-9}
3	0.0817	9.8541×10^{-8}
4	0.1158	2.1230×10^{-7}
5	0.2264	4.5738×10^{-6}
6	0.2413	9.8541×10^{-5}
7	0.2155	2.1230×10^{-4}
8	0.0676	4.5738×10^{-2}
9	0.0145	9.8541
10	0.0042	2.1230×10^{2}

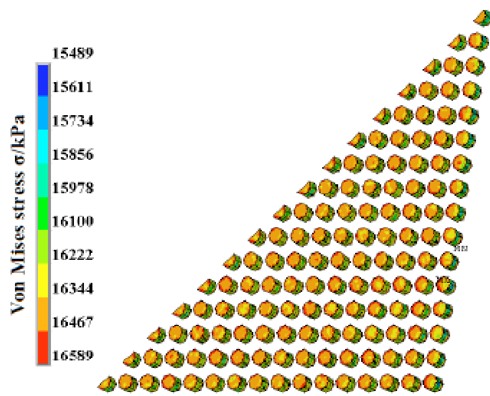

Fig. (3). Von Mises stress distribution of indium bumps array with 32×32 format.

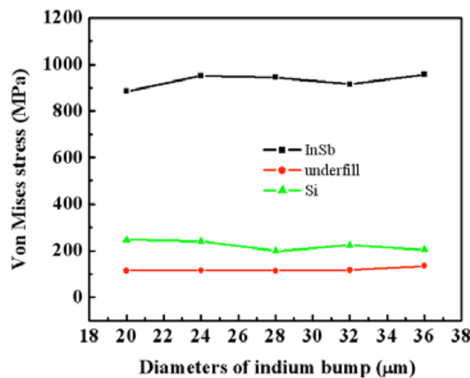

Fig. (4). Von Mises stress maximum values of 32×32 InSb chip as a function of InSb thickness with varied indium bump standoff height.

The glass transition temperature of the selected underfill is 408K, and the curing process is also operated at 408K for some time period, at this temperature, no residual stress is assumed to exist within the package. When temperature of 32×32 InSb IRFPA is gradually reduced from 408K to 77K in 71 seconds, Von Mises stress distribution of indium bumps is illustrated in Fig. (**3**). The Von Mises stress differ-

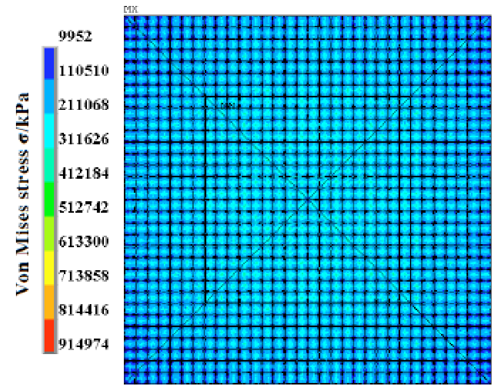

Fig. (5). Von Mises stress distribution of InSb chip bottom surface.

ence (1.1MPa) among indium arrays is so small that the Von Mises stress distribution is assumed to be uniform. The maximal Von Mises stress locating on the indium bump top surface locating at the twelfth row and eighth column intersection. Apparently, with the underfill dispensed among the gap between InSb chip and Si ROIC substrate, the stress in indium bump array redistributes, and its distribution is well uniformed.

In order to learn the effect from the indium bump diameter to Von Mises stress and its distribution in InSb chip, here a typical structure with InSb thickness 8μm, indium bump thickness 24μm is selected. While taking account of manufacturing precision the diameters of indium bump reduces from 36μm to 20μm in step of 4μm, the simulation results are shown in Fig. (**4**). With indium bump height is fixed at 24μm, the maximal Von Mises stress in the InSb chip fluctuates at 900Mpa, it seems that the stress is not dependent on the indium bump diameter, and the stress in underfill and Si ROIC also shows the similar varying tendency. Compared with the 8×8 InSb IRFPA array with underfill, the underfill is described with linear elastic properties, in a 32×32 InSb IRFPA array with viscoelastic properties underfill, the stress dependent on indium bump diameter is not obvious. So in the simulation process, omitting the underfill curing effect is not accurate, especially in larger indium bump diameter range.

In the whole InSb IRFPA detector, the maximal Von Mises stress, about 900MPa, appears on InSb chips edges, which is farthest to the neutral point, and is vertical to InSb top surface, the minimal Von Mises stress, about 16MPa, locating in indium bump array, and the stress in underfill encapsulant is about 114MPa, almost 7 times of that in indium bump array, this is not proportional to the support area, though their Young's modulus, Poisson's ratio, and coefficient of thermal expansion are comparable, the stress in Si ROIC is about 200MPa, slightly larger than that in underfill. All these are distinct from the Von Mises stress distribution in 8×8 InSb array detector without underfill, where the Von Mises stress distribution in all the contacting areas is uniform and concentrated, and its maximal stress is also located in contacting area between InSb chip and indium bump.

When indium diameter, height and InSb chip thickness are set to 32μm, 24μm, and 8 μm, Von Mises stress distribution of InSb chip, underfill and Si ROIC is shown in Figs. (**5-7**), respectively. Apparently, Von Mises stress existing on

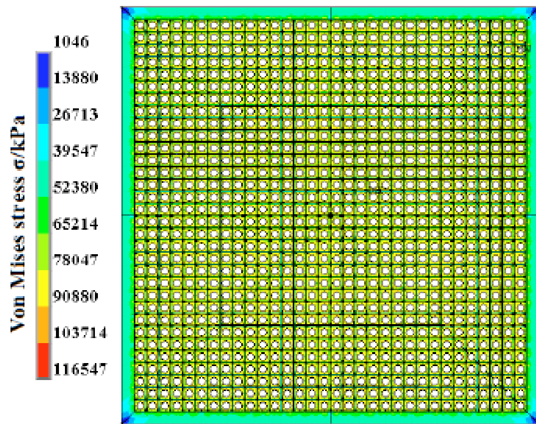

Fig. (6). Von Mises stress distribution of underfill top surface.

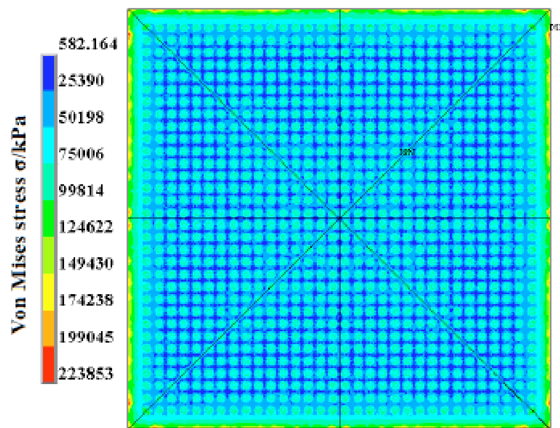

Fig. (7). Von Mises stress distribution of Si-CMOS readout integrated circuit.

contact areas between InSb chip and indium bumps is concentrated and uniform, its stress value is about 350MPa, larger than that of its surrounding areas. The maximal stress value about 915MPa situates at the edge far away from neutral point, where the InSb chip is confined by its surrounding underfill encapsulate and does not shrink freely. The minimal stress value about 9MPa locates on the trough intersection zones. There is an obvious stress gradient from contact section center to non-contact region.

Von Mises stress distribution in underfill is shown in Fig. (**6**). On the whole region under InSb chip, the stress distribution is uniform, and its stress value is about 80MPa, but around indium bump octahedral shell, the stress is apparently enlarged with maximal value 116MPa, and its minimum appears on the intersect region of convex triangular prisms, which is made of underfill locating in the troughs etching in InSb chip for isolating the neighboring detector cells. At the four corners of underfill top surface, Von Mises stress is small and is about 1MPa, here the underfill can shrink freely. Compared with indium bump array, apparently the underfill bears most thermal strain, for its stress is almost six times as large as stress in indium bump array.

Von Mises stress distribution in Si ROIC is almost concentrated strongly on the contacting areas between indium bumps and Si ROIC, around the contacting areas, the Von Mises is so small that it is ignorable, besides, on the quadrilateral borders of Si ROIC top surface, there are several non-continuous spots where Von Mises stress are the largest, especially near the corner of Si ROIC top surface, just as shown in Fig. (**7**). This is distinctly different from the stress distribution in the structure without underfill, where the stress distribution on the quadrilateral borders of Si ROIC top surface is ignorable [16].

CONCLUSIONS

Crack appearing in the InSb chip limited the InSb IRFPA final yield. Based on finite element analysis, impacts on Von Mises stress and its distribution in the InSb IRFPA from the structure parameters, including indium bump diameters and heights, are completely discussed in this manuscript. Simulation results show that the maximal Von Mises value existing in InSb chip is almost not dependent on indium bump diameters, and are mainly determined by standoff height, when the indium bump height is over 15μm, the stress reduces slowly with decreased standing off height. When the InSb IRFPA format increases from 8×8 to 32×32, the maximal Von Mises stress increases from 500MPa to 900MPa, which is almost twice over.

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