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Pseudo-Failure Impacts on ESD Robustness in Integrated Circuits I/O Ports by the Parasitic Capacitance

Shen-Li Chen* and Hung-Wei Chen

Department of Electronic Engineering, National United University, MiaoLi City 36003, Taiwan

Abstract: Semiconductor components are commonly electrostatic discharge (ESD) sensitive. The ESD event would usually cause a harm or destruction of the devices. Due to the requirement of circuits' reliability, the test for ESD robustness is necessary for almost all the product of integrated circuits. But during the test of ESD zapping, the test pin may temporary store ESD zapping charges. These stored charges will temporary cause shifting of the I-V characteristic curve of the test pin. And, it will seriously influence the ESD test results. Therefore, the electrostatic discharge (ESD) properties of the IC products in terms of the internal parasitic capacitance of the test pin are investigated in this paper. Eventually, it is found if the parasitic capacitance of the test pin is over 10-pf, the ESD test results may be not correct. We find, by suitable adjustment, the delay time between the ESD zapping and the measurement of I-V characteristic curve, a more correct result can be obtained. Therefore, it can correct the mistake made by parasitic capacitance in ICs and have a reliable ESD test result.

Keywords: Electrostatic discharge (ESD), ESD failure threshold (V_{ESD}), human-body model (HBM), parasitic capacitance, positive-to-VSS (PS) mode, pseudo failure

1. INTRODUCTION

Moore's law drives silicon ULSI technology to continuous progress. In 1996, the channel length was 0.35-μm, and in 1999 the channel length was scaled down to 0.18-μm. Today, the channel length of advanced CMOS IC is less than 22-nm [1-5]. With the channel length continue to scale down, the size of each transistor is also scaled down. But the density of IC is increased, such as; the density of DRAM is more than 1 G bits per chip. Same as the scale down of the channel length, the width of gate, the thickness of gate oxide, and the junction depth of source/drain are also reduced [6-11]. All of these reductions will cause decrease in the immunity to prevent the damage from the electrostatic charge. Thus, with the progress of IC technology, the robustness of ESD of IC product is lower than the early days [12-16]. However, today, all the IC products should still pass the minimum requirement of ESD test.

Integrated circuit (IC) component reliability relies on a standards-based evaluation. Commonly, the pass threshold of Human Body Model (HBM) in ESD standards for the commercial product (gate length ≥ 0.25-μm) is always set to be the ESD failure threshold (V_{ESD}) greater than 2-kV [17-19]. But, according to our test results, if we follow this condition to do the test, we find some products fail to pass the test. However, if we redo the same test after a period of time totally different results may come out.

This means we may have judged in error at the first time. There must have certainly been a factor affecting the test result. According to our experience, this is very often happens in mixed-mode or analog IC products. This paper proposed some experiments to make sure the reason why this happens and proposed a procedure to prevent the error in judgment.

2. EXPERIMENT DETAILS

In the ESD immunity level testing, we used a KeyTek ESD test machine shown in Fig. (**1**), the test waveform being confirmed the MIL-STD-883 EOS/ESD test standard [20]. The ESD test model was Human Body Model (HBM) and the maximum stress voltage can be up to ±8000-V. According to the test standard ANSI/ESDA/JEDEC JS-001 component level [21], the I/O pin, under test, must reference to VSS and the other non-test pin must float. And, we only use the positive-to-VSS (PS) mode for test. The test arrangement is shown in Fig. (**2**).

In order to gain a correct ESD testing data, many efforts in a test machine is reported in some patent literatures [22-27]. Authors in [22] proposed a design of ESD tester, on providing a physical contact while testing. And, how to perform an undistorted HBM and machine-model (MM) characteristics on ESD testers is revealed in [23]. Steven E. Marum *et al.* in [24] announced the ESD tester will generate an ESD event by providing an ESD test signal having a leading pulse and a trailing pulse. In [25] the authors present a method and procedule for calibrating an ESD tester. Furthermore, a running average of test measurements for the uniquely identified ESD device is adopted in a tester in [27].

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Fig. (1). An ESD test machine (KeyTek Zapmster 7/4).

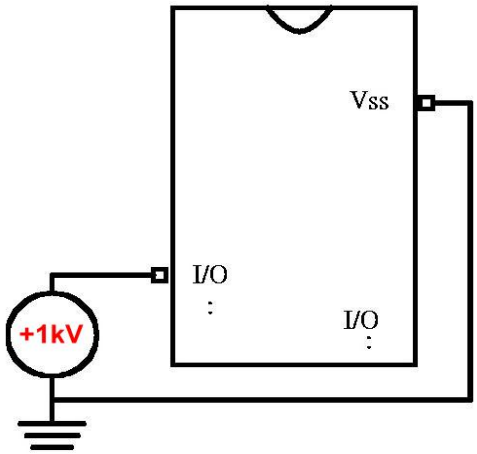


Fig. (2). Test arrangement of an ESD testing (PS mode).

In Table **1**, four different types of IC products are selected for experiments. The IC-1 is a commercial echo voice signal processing IC, IC-2 is a 10-bit 5-MHz ADC, and IC-3 is a 128-K bytes flash memory IC. And, IC-4 is a 256-K × 16-bit EDO DRAM. All of these four ICs are made by 5V CMOS technologies.

Before the ESD test, we use an HP4284A LCR meter (20-Hz ~ 1M-Hz) to measure the external equivalent capacitance of all the test pins. The VSS pin is used for the reference. This is to make sure the validity of the measured results. The other measuring conditions are: the measure frequency is 5-MHz, the signal level is 1.00-V, and length of test cord is 1 meter. Then, we select different order of magnitude of the capacitance from these four ICs to endure the ESD test. This is to find the relationship of pin capacitance with the critical failure voltage. Table **1** shows the selected pins for ESD test.

There are two methods that are used for this test. Method I: (a) measure the I-V curve of a test pin, (b) do an ESD zap test, (c) measure the I-V curve of the test pin right after the ESD test, (d) compare the measured I-V curves in (a) and (c). Method II: (a) measure the I-V curve of a test pin, (b) do an ESD test, (c) delay 1 second after the ESD test then measure the I-V curve of the test pin, (d) compare the measured I-V curves in (a) and (c).

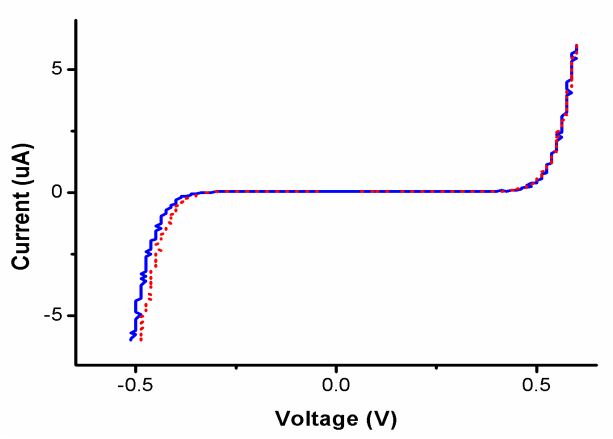
Then, we used the test results of Method II to find the relationship between the delay time and V_{ESD}. The Pin 2 and Pin 7 of A/D converter (IC-2) is selected as test pin for their large parasitic capacitance. The test voltages for HBM test are in the range of 500V~ 8000V and changes 500-V per step. The quantity of I-V draft is selected as the failure judge condition. That is, for sensing leakage current fixed at 1-μA [28-30], compare I-V curves before and after HBM test, if the voltage change is over ±30% ($\Delta V_{change} > \pm 30\%$), then this pin is judged as failed the HBM test at this zapped level. Once the test pin fails the test, the delay time is increased 100-msec, and the test is done again manually to make sure the I-V curve has failed.

3. RESULTS AND DISCUSSION

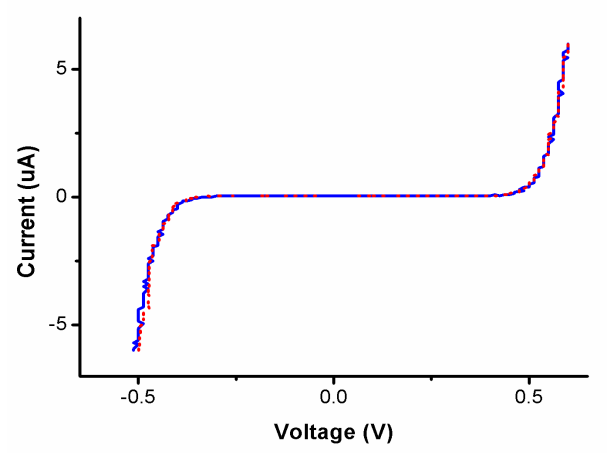
The HBM +1 kV ESD test results of IC-1 Echo IC are shown in Fig. (**3**) and Fig. (**4**). The I-V curves of Pin11 before and after ESD test are shown in Fig. (**3**) and Fig. (**4**) for Pin 13. The sub-figure (a) is the result with delay time is set to zero, and (b) with delay time is set to 1 second. From Fig. (3a) we can find the I-V shift is somewhat obvious, and, from Fig. (**3b**) the voltage draft disappeared. Then, we select Pin 13 (which has large parasitic capacitance pin) to do the same test. From Fig. (**4a**) the draft is worse than Pin 11. But, from Fig. (**4b**), the same with Fig. (**3b**), no draft is observed. Thus, we found: (1) all the test pins are not damaged by the ESD test, (2) the reason of voltage draft is that it comes from

Table 1. The selected pins for ESD test.

IC Model	Pin No.	C (pf)
IC-1 (Echo sound processor)	11 (REQ/DEL1)	31.5
IC-1 (Echo sound processor)	13 (SDATA/DEL3)	220.8
IC-1 (Echo sound processor)	28 (LPF1 IN)	7.6
IC-2 (A/D converter)	2 (DB0)	307
IC-2 (A/D converter)	7 (DB5)	307
IC-3 (Flash memory)	12 (A0)	5.0
IC-4 (DRAM)	16 (A0)	5.5



(**a**)



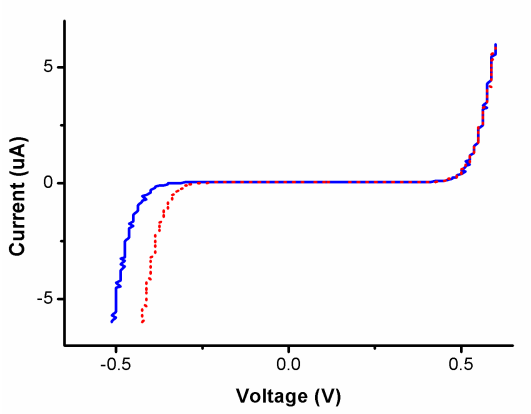
(**b**)

Fig. (3). HBM +1kV ESD test results of the Echo IC(IC-1)---Pin 11. (**a**) Delay time is set to zero; (**b**) Delay time is set to 1 sec (before zapping: blue solid line; after ESD zapping: red dot line).

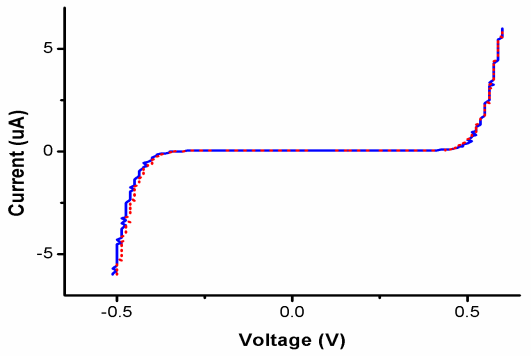
the temporary storage of pin parasitic capacitance. (3) this temporary charge storage effect will lead to a wrong judgment of the ESD evaluation, if the pin parasitic effective capacitance is obvious and large. We, then, select another pin (the pin 28) with a small pin parasitic effective capacitance (7.6-pf) for the same test and the results show no voltage draft as in Fig. (**5**).

In order to make sure other type of IC will have the same effect, we select the A/D converter (IC-2) to do the same test. The data I/O pin 2, which have greater parasitic capacitance (307-pf) than the IC-1 pin 13. The test results are shown in Fig. (**6**). Because of the capacitance is the greatest, thus the I-V curve shifting is also very obvious, as shown in Fig. (**6a**). And, no draft is found if the pre-charge is leaky by a delay time, as shown in Fig. (**6b**).

Another type of ICs: flash memory (IC-3) and DRAM (IC-4) are also choice for the ESD test to confirm the parasitic capacitance effect. Fig. (**7**) shows the test results of IC-3 Pin 12 with the effective capacitance of 5.0-pf and Fig. (**8**) shows the test results of IC-4 Pin 16 with the effective capacitance of 5.5-pf. All the test results show no I-V curve



(a)



(b)

Fig. (4). HBM +1 kV ESD test results of the Echo IC(IC-1)---Pin 13. (**a**) Delay time is set to zero; (**b**) Delay time is set to 1 sec (before zapping: blue solid line; after ESD zapping: red dot line).

shifting as before and after ESD zapping (the delay time is set to zero). According to these test results, we can find if the pin effective parasitic capacitance is over 10-pf, the ESD test may have wrong judgment if the traditional test method is used. And, of course, for the ESD test, the pin with the less effective capacitance the less the wrong judgment for it has less temporary charge storage.

4. RESPONDING MODEL OF TESTING DUTS

When an IC DUT was performed the ESD testing which would do an ESD zap test and then measure the I-V curve of a test pin shown in Fig. (**9**). However, when an ESD transient or noise voltage is firstly applied to the test pin of an IC component, there was a parasitic capacitance that existed between this test pin and grounding, as shown in Fig. (**10**). When an increasing ESD voltage is applied to this pin, the capacitor (C_{pin}) shows a charging current and charges up. When the next step is applied for the I/V leakage measurement, if the voltage stored in this pin does not disappear, then the capacitor (C_{pin}) discharges in the opposite direction. Due to this, the parasitic capacitor, is able to accumulate electrical energy and it act likes a small battery. The charge on this C_{pin} capacitor is given as: $Q = C_{pin}V$. This charging (ESD zapping) and discharging (leakage I/V measurement)

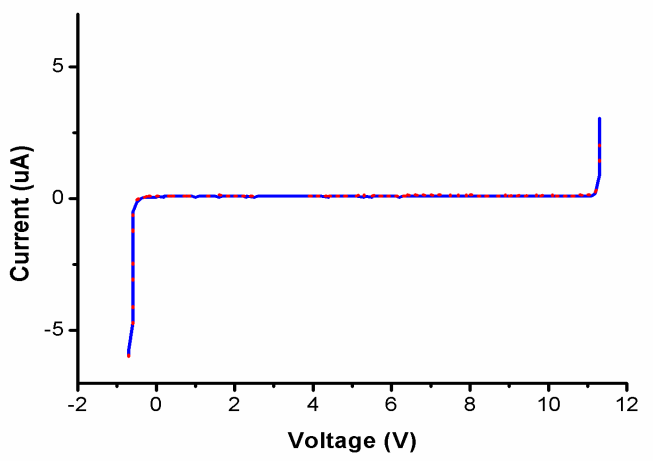
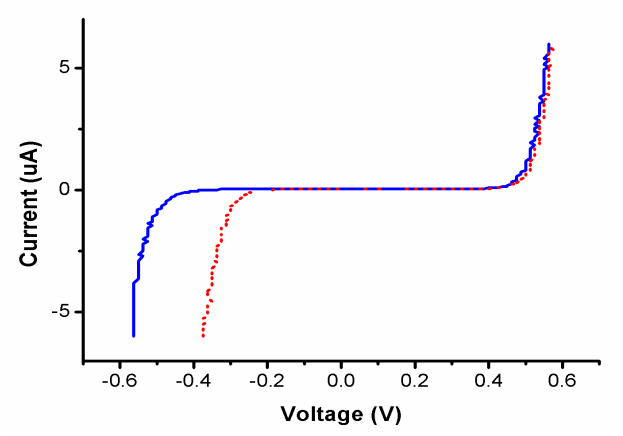
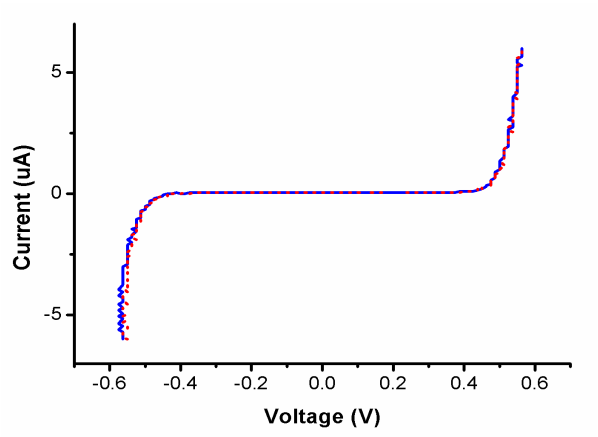


Fig. (5). HBM +1kV ESD test results of the Echo IC (IC-1)--- Pin 28 (before zapping: blue solid line; after ESD zapping (delay time is set to zero): red dot line).



(a)



(b)

Fig. (6). HBM +1kV ESD test results of the A/D Converter IC (IC-2) --- Pin 2. (a) Delay time is set to zero ; (b) Delay time is set to 1 sec (before zapping: blue solid line; after ESD zapping: red dot line).

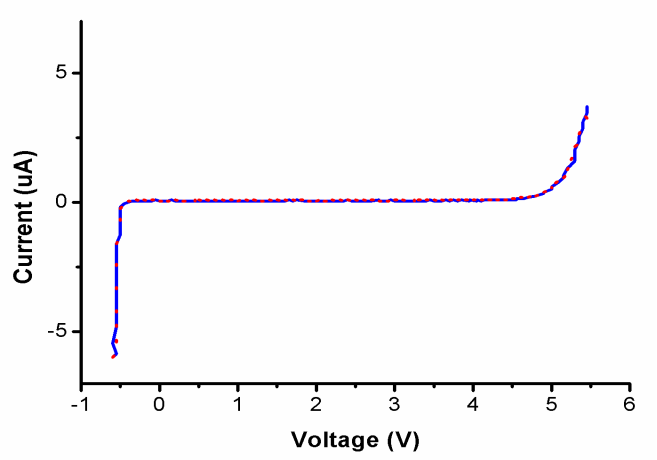


Fig. (7). I-V curves of the flash memory (IC-3) Pin12--- before zapping: blue solid line; and after ESD zapping (delay time is set to zero): red dot line.

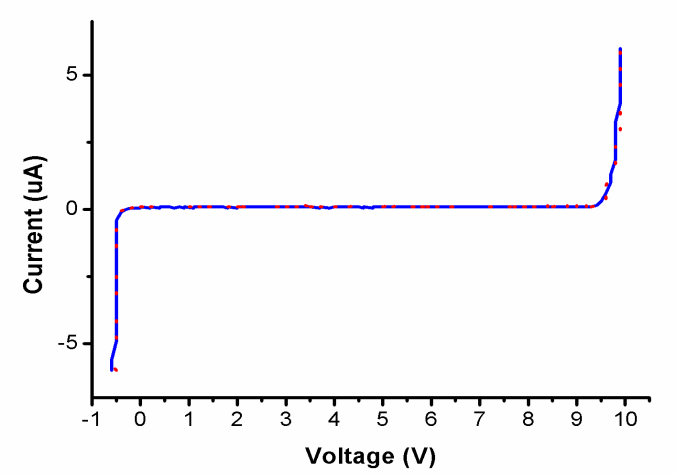


Fig. (8). I-V curves of the DRAM (IC-4) Pin16--- before zapping: blue solid line; and after ESD zapping (delay time is set to zero): red dot line.

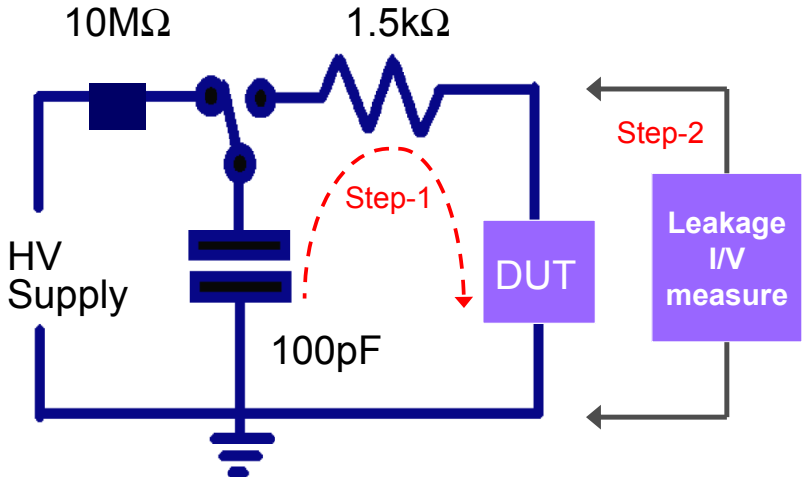


Fig. (9). Procedure steps illustration of an HBM testing for IC DUTs.

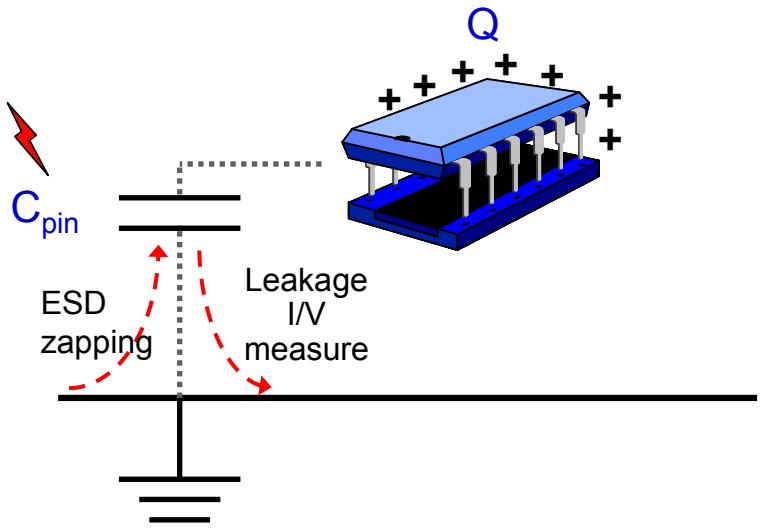


Fig. (10). An equivalent parasitic capacitance C_{pin} between the testing pin and grounding for an IC DUT.

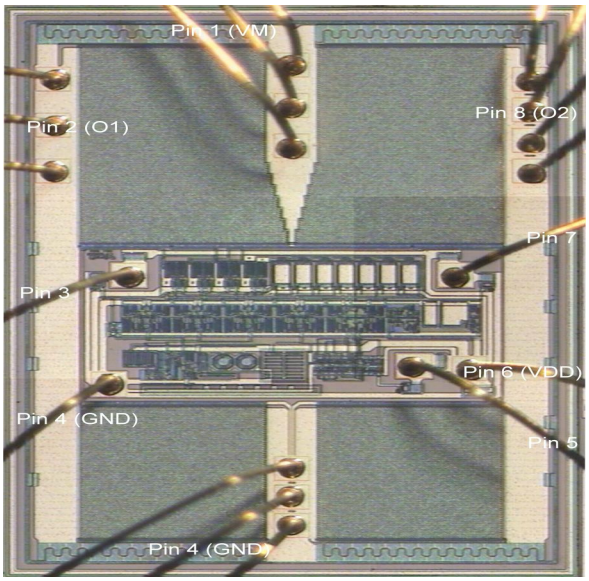


Fig. (11). Chip photograph of a selected power IC.

of this capacitor energy is never instant but takes a certain amount of time to occur, which known as its time constant RC_{pin}.

If an embedded resistor R is connected in series with this parasitic capacitor (C_{pin}) forming an RC circuit, the capacitor will discharge down gradually through the resistor until the voltage across the capacitor reaches zero. Nevertheless, the time, called the transient response, required for this to occur is equivalent to about 7 RC (~0.1% peak magnitude). So, as a parasitic capacitance of the testing pin is about 10-pf and the resistance of R is 100-MΩ (for the vacuum situation), then the 7 time constant is reached about 10-ms order.

5. CORRECTIVE AND VERIFICATION TESTING

The output pin of an analog power IC always has high parasitic capacitance. It is because of the power the IC needs to drive a large load, thus the output stage must use large silicon area to sink and source high current. For this type of IC, the ESD test draft effect will be significant. To confirm, we chose a power IC to do this ESD testing. As shown in Fig. (**11**), where the layout area is 600-μm × 600-μm for the Output1 (O1) or Output2 (O2) port. The test pins are the O1 or O2 pin for zapping +500 V HBM. Fig. (**12**) shows the results of I-V curves with delay time zero, Fig. (**13**) the delay time is 18 minutes, and Fig. (**14**) the delay time is 23 minutes. For the I-V curves of Figs. (**12-14**), the blue line is for after the ESD test, and the purple line is for before the ESD test. If the delay time is zero, after ESD test, the output pin is a short circuit and this pin will be judged as a fail. If the delay time is 18 minutes, after ESD test, the test result show voltage draft and this pin will be judged as a fail. However, if the delay time is 23 minutes, no voltage draft occurs, this pin is judged as a pass. From the experiments above, we found that the select of delay time for ESD test is critical and strongly dependent on the test pin parasitic effective capacitance.

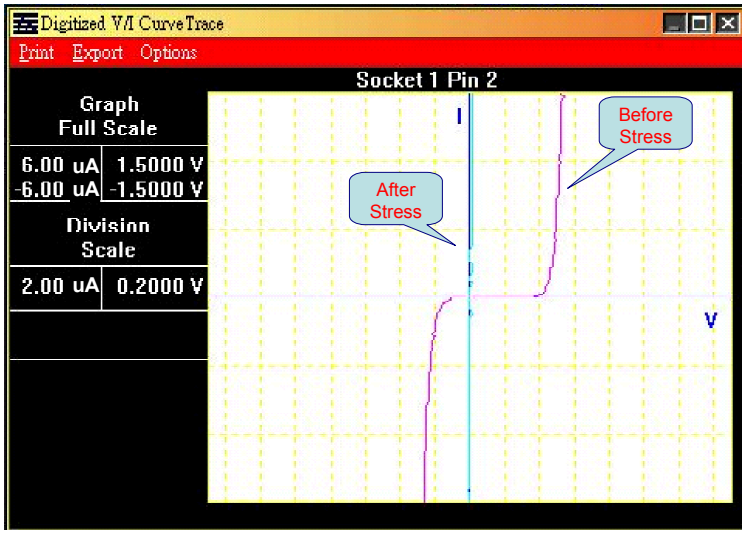


Fig. (12). I-V curves of a power IC (before and after ESD test)--- delay time is 0 minute.

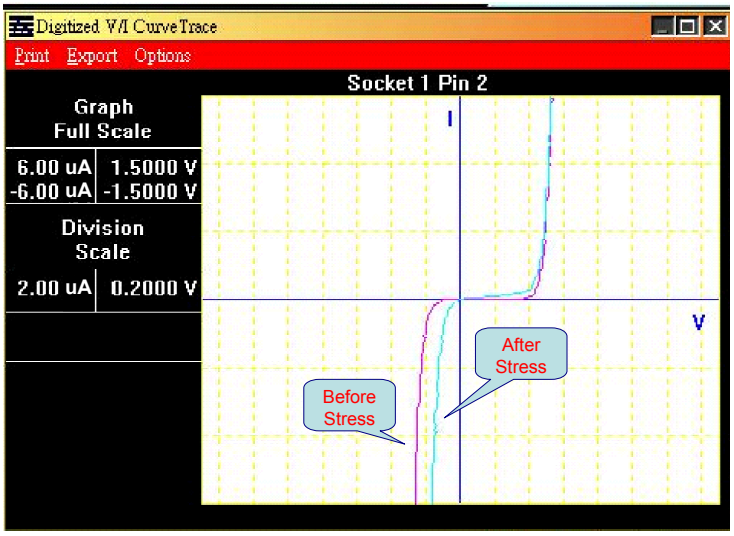


Fig. (13). I-V curves of a power IC (before and after ESD test)--- delay time is 18 minutes.

In order to find the suitable delay time for ESD test, we select Pin 2 and Pin 7 of the above mentioned A/D converter IC (IC-2) that has serious draft effects to do a more complete experiment. Finally, the experiment results are shown in Table **2**. For Pin 2, if the delay time is over 0.8-sec, the ESD failure threshold (V_{ESD}) can be correctly measured. For Pin7, the delay time must be over 0.5-sec. The test equipment is a Keytek ESD Tester, as shown in Fig. (**1**). The standard test procedure for such ESD tester is specified as follow: (1) set-up ESD test and do the I-V curve evaluation right away; (2) delay 1 second (original setup), do the next ESD test again. Every time after the ESD test, the I-V curves are compared to make Pass/Fail decision. Thus, we can see this standard procedure may cause wrong decision for the temporary charge storage in a large parasitic capacitance. That is, the delay time should be careful examination to get a right critical value for ESD robustness evaluation.

Based on the experiments mentioned above we propose that the ESD test procedure should be modified as follow. For the general purpose IC, after the ESD test, before measuring the I-V curve, at least a 0.9 second delay is necessary. After I-V measure, must delay by at least 0.1 second before the next cycle of ESD test. Thus, we can have more reliable result and less speed penalty. Nevertheless, we have used this modified procedure on the Keytek ESD tester, with the increase of the delay time before the I-V measurement and ZAP interval time, the test pin have enough discharge time, a satisfactory test report can be obtained.

6. DISCUSSION ON CURRENT & FUTURE DEVELOPMENTS

In this study, the pseudo-failure impacts on ESD evaluation is proposed for the first time in ICs HBM testing. If the parasitic effective capacitance of I/O pin is too large, the I-V curve, after ESD test, may distort too much and may give a wrong result. By suitable adjustment of the delay time, we succeeded in removing this charge storage effect and enabled

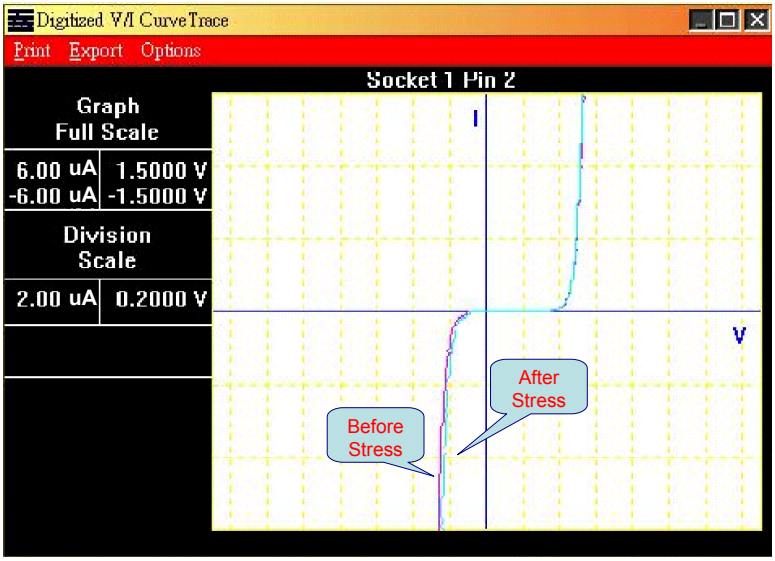


Fig. (14). I-V curves of a power IC (before and after ESD test)--- delay time is 23 minutes.

Table 2. Effect of delay time vs. ESD failure threshold (V_{ESD})--- the A/D Converter IC (IC-2) Pin2 and Pin7.

Pin #	Delay Time	V_{ESD}	Pin #	Delay Time	V_{ESD}
2	0 msec	1.5 kV	7	0 msec	0.5 kV
	100 msec	1.5 kV		100 msec	0.5 kV
	200 msec	1.5 kV		200 msec	0.5 kV
	300 msec	1.5 kV		300 msec	0.5 kV
	400 msec	1.5 kV		400 msec	1.0 kV
	500 msec	1.5 kV		500 msec	5.5 kV
	600 msec	2.0 kV			
	700 msec	2.0 kV			
	800 msec	4.5 kV			

a more precise ESD test. With a complete study of the I-V draft with the parasitic effective capacitance of I/O pin, we propose a new ESD test procedure that is suitable for standard ESD test without the penalty of test speed and with an accuracy of testing data for the future industrial applications.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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