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Design of System for Electromechanical Equipment Condition Monitoring in Real-time Based on DSP and CPLD

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Abstract: A multi-parameter monitoring system has been designed for mechanical and electric equipment based on DSP and CPLD. Designing methods for hardware and software are introduced in this paper. As in the system, powerful capability for numeric operation of DSP is used to deal with real-time data, while CPLD is held responsible for logic control. Therefore, by combining DSP and CPLD, malfunction can be observed and alarming signal can be provided in due time.

Keywords: CPLD, DSP, real time monitoring, USB interface.

1. INTRODUCTION

In the industrial field, the implementation of real-time monitoring and displaying of important parameters (such as pressure, temperature, liquid level, speed, vibration, *etc*.) regarding the equipment are very necessary. But at present, the monitoring of electromechanical equipment is either single parameter monitoring or is too complex. In this paper, a real-time monitoring system is designed. It makes use of DSP-TMS320LF-2407A as a processor, uses CPLD to determine logic control and communicates with the host computer *via* USB interfaces. The system can automatically complete acquisition, hold storage for various parameters and intuitively display the result in digital or curve. It can enable the staff to master the working conditions of the equipment in a timely manner and also the predictive maintenance of the equipment can be realized beforehand. This can further enhance the economic efficiency of the enterprises.

2. GENERAL SCHEME DESIGN

In this system, modular design method is adopted. The structure diagram is showed in Fig. (**1**). It mainly includes sensor module, signal acquisition and processing module, the D/A conversion module, USB communication module, power and it's logic control module and a necessary computer display.

The physical quantities such as pressure, temperature, speed and so on are converted into electric signals by the sensor portion. Its acquisition and processing module is then responsible for receiving the sensor signals, amplifying, shaping, A/D converting, filtering and other processing. Then, these signals are sent to the computer through the USB interface and are displayed in graphical, tabular or digital form. Simultaneously, the computer sends a control signal which is transferred by the acquisition and controlling module to the D/A conversion. Finally, it acts on the controlled parts to reach the conformity of purposes. Taking the future expansion of demands of the system into account, 8-way switches of input capture and output control are also added to the design.

3. HARDWARE DESIGN FOR SYSTEM

According to the actual requirements of the industrial site, hardware realizing of the system includes the DSP minimum hardware system, logic control of CPLD, extended memory interface, frontal and backward channels, USB communication interface, power source and so on. Hardware realizing block diagram of this system is shown in Fig. (**2**). Then several main components are introduced.

3.1. Data Acquisition and Processing

The main function of the data acquisition and processing module is to determine data acquisition, pretreatment, storage, upload, *etc*. At the core of the module device is a DSP (digital signal processor), whose primary task is to analyze and process the signal from forward-channel according to certain algorithms so as to form various effective data to meet the preset functions, and then the processed results are forwarded to the backward channel. Forward channel includes such circuit responsible for processing 16-channel analog signals, shaping and amplifying 8-way pulses and controlling the outputting of extension, inputting the segregated circuits of 8 group switches, *etc*. Backward channel includes output information of 4-channel analog and extended 8 group switches.

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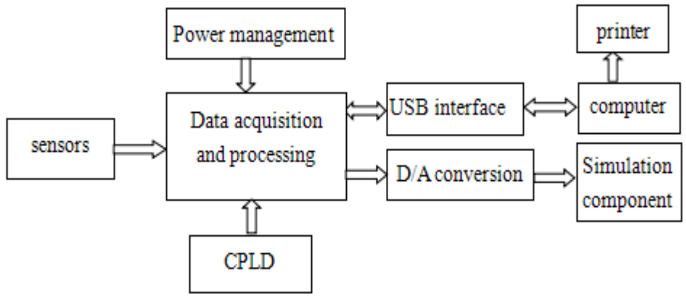

Fig. (1). Structure of the system.

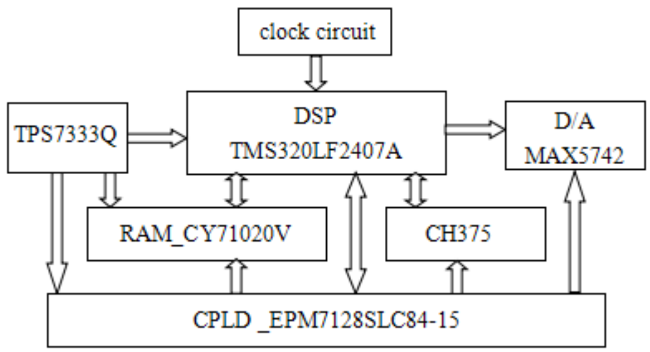

Fig. (2). Hardware realizing of the system.

According to the system design requirements, the DSP-TMS320LF2407A of company TI is used. It has a watchdog timer module and an internal 10 bit A/D converter module. Therefore, the design of the peripheral circuit is simplified. At the same time, the reliability and the programmability of the system are improved. In addition, it possesses other characteristics such as high integration, large program storage capacity and fast switching speed for the A/D module, *etc*. [1, 2]

3.2. External Data Memory Expansion

The TMS320LF2407A has single port SRAM with 2K bytes, dual port DRAM with 544 bytes and FLASH program memory of 32Kx16 bit. The program memory space and the data storage space of the chip can be extended to 64K bytes, and so is the I/O space. Program memory of the chip can meet the requirements of the system. Considering the requirement of the DSP power and memory access speed, a parallel memory of 32Kx16 bit is expanded in the design to ensure adequate data storage space. It is CY7C1020V.

The parallel memory (CY7C1020V) of company CYPRESS is a high performance CMOS memory. Its power supply voltage is +3.3 V. This is same as the DSP chip power. Minimum access time of the parallel memory is l0ns. The parallel memory (CY7C1020V) has a special function of being in a low power state when not selected. This can reduce power loss. Thus, the system is energy-efficient [3].

3.3. Application of CPLD

CPLD/FPGA and other logic devices have many characteristics such as high integration, on-site programming, good expansibility [4], which can better meet the DSP requirements of the peripheral digital interface circuits. In this system, EPM7128SLC84-15 produced by Altera Corporation of the United States is selected as the peripheral device of TMS320LF2407A for SRAM, D/A converters and USB interface so as to determine the controlling functions for counters, address decoders and logic controlling. EPM7128SLC84-15 is a programmable device on line. This device has four dedicated inputs, 64 general-purpose I/ O pins and 128 logical units. Its advantage lies in the fact that it can be programmed repeatedly up to a hundred times not requiring the removal of the chip directly while programming on the circuit board [5]. A hardware description language VHDL programming is used, which greatly simplifies the decoding circuit. Essentially, some logic control of CPLD involves the usage of the counter. The division of the clock frequency following a VHDL program can be used as an example to illustrate the application of CPLD.

```
entity count512 is                    - - -entity illustration
  port(clk:in std_logic;                 - - -port illustration
          c0,c1,c2,c3,c4,c5,c6,c7:out std_logic);
    end count512;
    architecture rtl of count512 is              - - -structure
```

```
    signal count_512_v: std_logic_vector(8 downto 0);
    signal count_8_v: std_logic_vector(7 downto 0);
begin                                   - - -signal assignment
    c0<=count_512_v(0);
    c1<=count_512_v(1);
    ………………………
    c7<=count_512_v(7);
process(clk)                            - - -process
    begin                               - - -start counting
       if(clk'event and  clk='1')then
       if(count_512_v="111111111")then
          count_512_v<="000000000";
       else
          count_512_<=count_512_v+'1'
       end if;end if;                   - - -end
    end process;
end rtl;
```

3.4. USB Interface

Universal Serial Bus (USB) is a synchronous transmission serial interface that is based on the token. It is rapid and bidirectional and can be a hot swap. Nowadays, almost all of the industrial computers are equipped with a USB interface. In this design, CH375 of Nanjing qinheng electronics company is used. It conforms to a USB2.0 protocol. It is a universal interface chip of USB bus. al the local end, CH375 has an 8 bit data bus and reading, writing, chip selects controlling line and interrupts output. It can be conveniently attached to the system bus of Single chip microcomputer/DSP/MCU controller and so on. In USB host mode, CH375 also provides a serial communication mode. It can be connected with the SCM/D-SP/MCU by serial input, serial output and interrupt output. Moreover, CH375 USB host mode supports a variety of commonly used full speed devices of USB. The external SCM /DSP/MCU can communicate with USB device by CH375 according to the corresponding USB protocol.

3.5. Power-supply Module

Due to the different voltage grades of each module and certain requirements of the power on sequence, TPS7333Q is chosen as the power management chip. This chip is specifically developed for DSP. TPS7333Q is a low dropout linear regulator circuit with higher noise suppression ability to power source. It can not only convert the voltage from +5 V to +3.3 V but also provide a low level signal about 200ms as the reset signal for DSP chip.

4. SOFTWARE DESIGN FOR SYSTEM

The system software mainly comprises of the following functions:

(1) Data Acquisition: it is based on the control of the A/D conversion process, storing the converted data into the buffer of DSP and reading pulse number into the DSP with the aim of further processing.

(2) Data Processing: includes digital filtering of the data, frequency spectrum analysis, computation of characteristic quantities, correlation calculation of channel data, and treatment of the switch quantity and so on.

(3) Data Communication: forwards the processed data to PC through USB port and responds to data in accordance with the requirements of the PC at the same time.

(4) Result Analysis: through characteristic analysis, the most sensitive characteristic quantities of the working conditions are chosen by PC. At the same time, these characteristic quantities are stored and displayed. If there is any abnormality, alarming signal is given.

First, the system is initiated by configuring the interrupt settings to TMS320LF2407A system. By setting the configuration register SCRC1 (SCRC1 the = 0x00AC) of the system, the system operating clock frequency is determined and the associated interrupt flags are cleared . When the system's initialization is complete, all kinds of DSP modules are initiated, including timers, A/D conversion, general-purpose I/O ports, SPI ports, USB ports, *etc*. Then, an interrupt is opened to start the A/D converter and waits for the timer 1 interruption, reading the A / D converted data for writing to the corresponding data buffers, processing the data for digital filters; after that, it waits for timer 2 interruption to read the pulse count value, calling correlation algorithm to calculate the amount of system status, and the results are sent to the host computer. However, if the host computer has data requests, TMS32 0LF2407A is interrupted to respond to USB communication, sending data results to the host computer via the USB ports. A variety of characteristic quantities for running are monitored and displayed by the host computer so as to analyze the causes and implications for fault condition and forecast development trends.

In this paper, DSP software program is designed through hybrid programming in which C language combines with assembly language. Software for TMS320LF2407A is developed in CCS3.3 integrated environment [6, 7]. Module program of CPLD is designed in Quartus Π 5.0. Quartus Π 5.0 is an excellent development platform for CPLD. It comes with the basic logic block, IP function module, library parameter module, *etc*. It provides convenience for designers. The main program flow chart is shown in Fig. (**3**).

CONCLUSION

From the above-mentioned content, a new train of thought and solution is proposed for multi-parameter monitoring in real-time. DSP and CPLD are combined, communication with PC is achieved by USB, acquisition, processing and monitoring of various signals are obtained and abnormity is found in time. These solutions may provide reliable safeguards for the smooth running of the mechanical and electric equipment. This technology, however has already been put

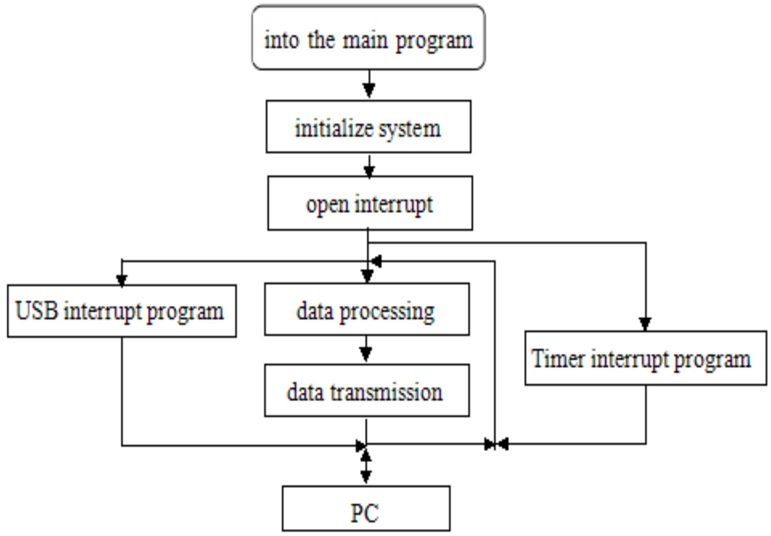

Fig. (3). Flow chart of main program.

to use in multi-parameter monitoring for rotating machines and has achieved good beneficial results.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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