

# An Investigation of Super-Threshold FinFET Logic Circuits Operating on Medium Strong Inversion Regions

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**Abstract:** Scaling supply voltage of FinFET circuits is an efficient method to achieve low power dissipation. Super-threshold FinFET logic circuits can attain low power consumption with favorable performance, because FinFET devices operating on medium strong inversion regions can provide better drive strength than conventional CMOS transistors. The supply voltage of the super-threshold circuit is much larger than threshold voltage of the transistors, but it is lower than normal standard supply voltage. In this paper, basic FinFET logic gates based on static logic, DCVSL (Differential Cascade Voltage Switch Logic), PTL (Pass Transistor Logic), and TG (Transmission Gate) logic styles operating on medium strong inversion regions are investigated in terms of power consumption and delay. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The simulation results show that super-threshold FinFET logic gates operating on medium strong inversion regions attain about 41% power reduction with a penalty of only about 23%.

**Keywords:** FinFET, low-power designs, medium strong inversion regions, super-threshold logic circuits.

## 1. INTRODUCTION

The total power consumptions in a modern CMOS circuit include three parts: static power dissipation caused by leakage currents of MOS devices, dynamic power dissipations caused by charging and discharging nodes of circuits, and short-circuit dissipations [1]. The short-circuit power losses due to a direct-path from supply voltage to the ground can usually be ignored. In modern integrated circuits (ICs), technology scaling increases their density and performance, resulting in large dynamic power dissipations [2]. Meanwhile, the aggressive scaling of MOS devices has greatly increased leakage power dissipations exponentially, because continued scaling reduces the threshold voltage, channel length, and oxide thickness [2]. Therefore, the aggressive scaling of IC device dimension has greatly increased both dynamic and leakage power dissipations.

With the increasing demand for battery-operated mobile platforms like laptops, and biomedical applications that require ultra-low power dissipations, low power designs have become more and more important. IC designers work hard on high performance with low power dissipation and small area [3-5].

Scaling supply voltage is an effective method to reduce power consumption, since the dynamic energy dissipation is reduced quadratically and leakage losses decrease linearly as supply voltage scales down [6-10]. For CMOS

circuits, sub-threshold circuits are one of the best solutions to achieve low energy consumption [6]. However, the performance of the sub-threshold circuits is much lower than these circuits operation on normal source voltages due to the exponential relationship between delay and supply voltage. Therefore, sub-threshold circuits only fit low-performance application [6, 7].

In recent years, the near-threshold circuits are presented [8-10]. The supply voltage of near-threshold circuits is slightly above the threshold voltage of the transistors [8]. Since near-threshold computing for CMOS circuits can reduce both dynamic power dissipations and leakage power losses, this region retains much of the energy savings of sub-threshold operation. Moreover, near-threshold circuits have more favorable performance than sub-threshold circuits because of larger turn-on currents. However, the CMOS near-threshold circuits are only suitable for mid-performance applications, because the MOS device of near threshold circuits operates on medium inversion regions.

With the aggressive scaling of CMOS device, the leakage current of the conventional CMOS circuits has increased significantly, so that leakage power dissipations are becoming the main source of power consumption [2]. Hence, it is necessary to develop novel devices. Among the recently reported novel devices, FinFET (Fin-type Field-Effect Transistors) device shows excellent performance and low-power characteristic, and has been proven as a promising alternative for the conventional CMOS device to realize continued scaling, because it can well suppress the SCEs (Short-Channel Effects) and the gate-dielectric leakage current [11].

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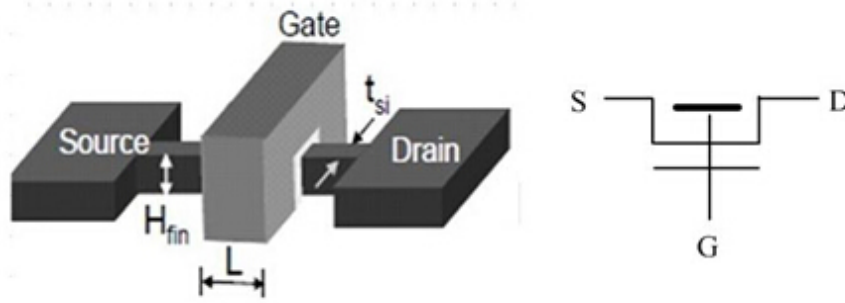


Fig. (1). The structure and symbol of FinFET.

In this work, an investigation for FinFET circuits using static logic, DCVSL (Differential Cascode Voltage Switch Logic), PTL (Pass Transistor Logic), and TG (Transmission Gate) logic styles operating on super-threshold regions is carried out. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology [12]. The supply voltage of the super-threshold circuit is much larger than threshold voltage of the transistors, but it is lower than normal standard supply voltage. As mentioned above, near-threshold circuits are not suitable for high-speed applications. Compared with the conventional CMOS, FinFET has higher turn-on current, and thus FinFET circuits can provide better drive strength. Therefore, FinFET logic circuits operating on medium strong inversion regions have more favorable performance than near-threshold circuits because of larger turn-on currents. Meanwhile, the super-threshold FinFET circuits retain much of the energy savings of near-threshold operation.

## 2. POWER & DELAY OF FinFET CIRCUITS

The FinFET with three-dimensional structure is shown in Fig. (1) [11]. The FinFET device consists of a thin silicon body. The thin silicon body is wrapped by gate electrodes, the thickness of which is denoted by  $t_{si}$ . The current of the FinFET device flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. As shown in Fig. (1), The FinFET is a double-gate device. Its two gates can either be shorted or independently controlled. The independent front and back gates of the FinFET can be achieved by etching away the gate electrode at the top of the FinFET channel [13, 14]. In this work, only SG (Short-Gate) mode is considered. The effective gate width of a SG FinFET is  $2nH_{fin}$ , where  $n$  is the number of fins, and  $H_{fin}$  is the height of fins. The wider transistors are only obtained by using multiple fins.

The simulation results for the I-V characteristics of 32nm n-type FinFET and conventional bulk NMOS are shown in Fig. (2). Compared with the conventional bulk NMOS transistor, FinFET device has high turn-on current, and thus fast switching speed. Therefore, FinFET logic circuits operating on medium strong inversion regions have more

favorable performance than conventional bulk CMOS because of larger turn-on currents.

As shown in Fig. (2), the FinFET device has larger sub-threshold slope than conventional bulk MOSFET because of the strong gate control over the channel. Compared with bulk MOSFET, the leakage of the FinFET device is reduced significantly.

PDP (Power Delay Product) metric provides a good compromise between power consumption and speed. The total power consumption ( $P_{total}$ ) is expressed as;

$$P_{total} = P_{dyn} + P_{leakage} = fC_L V_{DD}^2 + V_{DD} I_{leakage} \quad (1)$$

where  $C_L$  is the load capacitance,  $V_{DD}$  is source voltage,  $f$  is operation frequency, and  $I_{leakage}$  is leakage current of FinFET devices.  $P_{dyn}$  scales quadratically with the supply voltage. As supply voltage scales down,  $P_{leakage}$  is reduced linearly.

Assuming symmetrical P-type and N-type FinFETs, when the source voltage is larger than the threshold voltage, the delay of a FinFET inverter is;

$$t_d = \frac{KC_L V_{DD}}{(V_{DD} - V_{th})^a} \quad (2)$$

where  $K$  is a delay fitting parameter,  $a$  is velocity saturation parameter, and  $V_{th}$  is threshold voltage.

PDP is written as:

$$PDP = P \times t_d \quad (3)$$

Plugging (1) and (2) into (3) gives the PDP:

$$PDP = \frac{(fC_L V_{DD}^2 + V_{DD} I_{leakage}) KC_L V_{DD}}{(V_{DD} - V_{TH})^a} \quad (4)$$

## 3. FinFET CIRCUITS

Basic logic gates are important units in digital circuits, since they are used extensively in digital systems. Several basic FinFET logic gates using static logic, DCVSL, PTL, and TG logic styles operating on medium strong inversion regions and super-threshold regions are investigated.

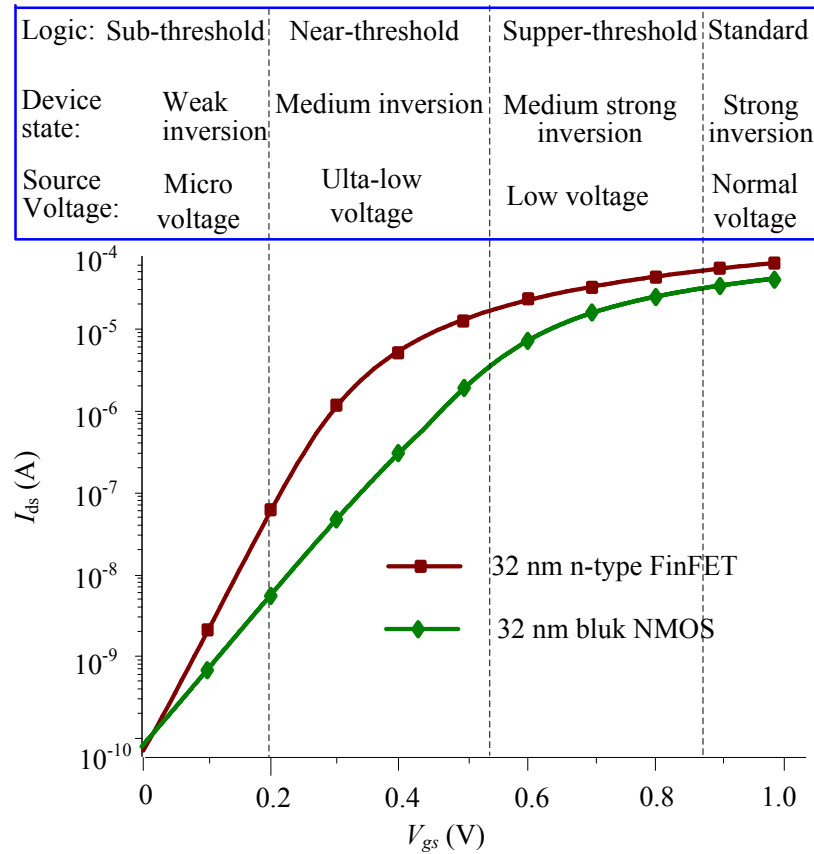


Fig. (2). I-V characteristics of 32 nm n-type FinFET and conventional bulk NMOS transistor.

The typical static complementary logic gates with the pull-up network (PUN) and the pull-down network (PDN) are shown in Fig. (3), whose structure is the same as static complementary CMOS.

The DCVSL family replaces the PUN of static FinFET logic circuits by a pair of cross coupled P-type transistors [1]. The basic FinFET gates based on DCVSL are shown in Fig. (4). Due to using only N-type logic blocks, it may consume less area. In addition, their positive feedbacks help speed up the transition.

PTL circuits consist mostly of N-type transistors, which lead to small area and capacitance, as shown in Fig. (5). Similar to CMOS PTL, the FinFET circuits based on PTL requires inverters to provide complementary inputs and enables rail-to-rail swing. PTL can be used to build some complex gates very effectively especially for the XOR and XNOR circuits.

The transmission gate (TG) logic circuits are realized by replacing N-type transistors with transmission gates in PTL circuits, as shown in Fig. (6). The transmission gate (TG) logic circuits use double transistors to overcome the threshold loss of PTL circuits. Similar to PTL, TG requires also additional inverters to provide complementary inputs. TG can also be used to build some complex gates very effectively especially for the XOR and XNOR circuits.

#### 4. COMPARISONS OF DIFEERENT LOGIC STYLES

HSPICE simulations have been carried out for the four basic logic gates based on static FinFET logic, DCVSL, PTL, and TG logic with different voltages from low voltage to normal standard voltage, where the channel of the FinFET devices operate on medium strong inversion regions and strong inversion regions, respectively. All circuits are simulated with HSPICE at a PTM 32nm FinFET technology.

In order to simulate the work environment of basic gates, the testing platforms for single rail logic circuits (Static FinFET logic, TPL, and TG logic) and dual rail logic circuits (DCVSL) are shown in Fig. (7) and Fig. (8), respectively. The power dissipations of the basic logic gates in the dotted box shown in Fig. (7) and Fig. (8) are tested. In order to assure fair comparisons, the two inverters are paralleled after all outputs to act as load capacitances, and the same input is given to these gates. An optimization of fin number considering delay and power has been carried out for all the four gates.

The propagation delay of a gate is expressed as:

$$t_{\text{delay}} = \frac{t_{\text{pLH}} + t_{\text{pHL}}}{2} \quad (5)$$

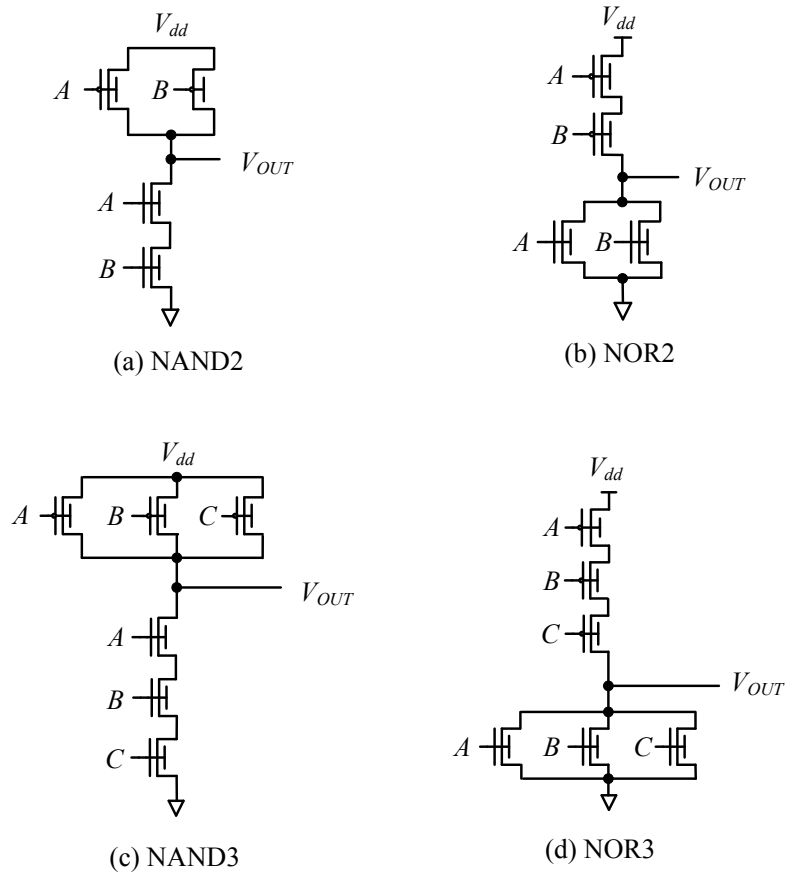


Fig. (3) Static FinFET gates.

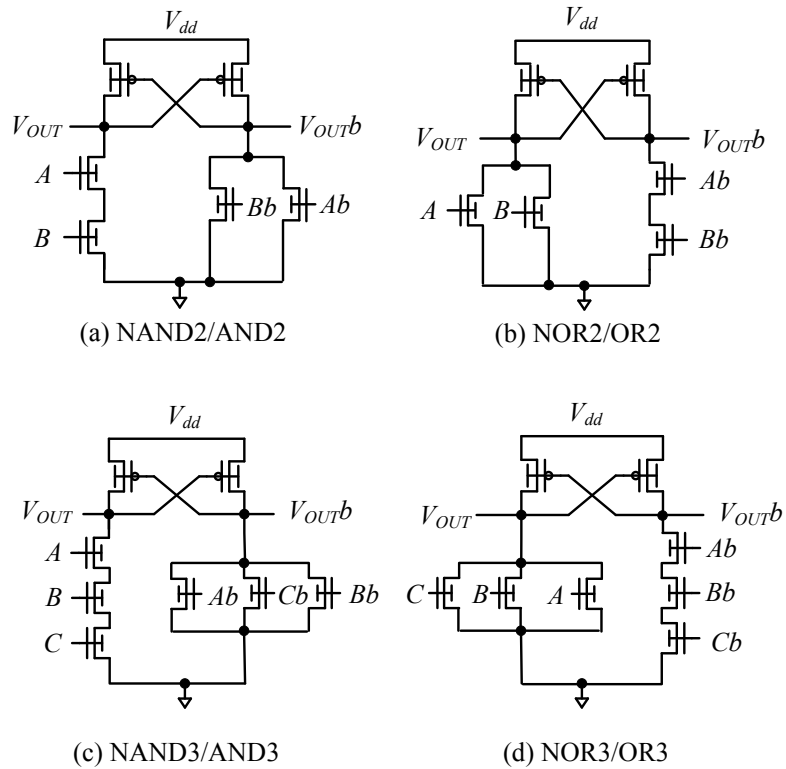


Fig. (4). DCVSL FinFET gates.

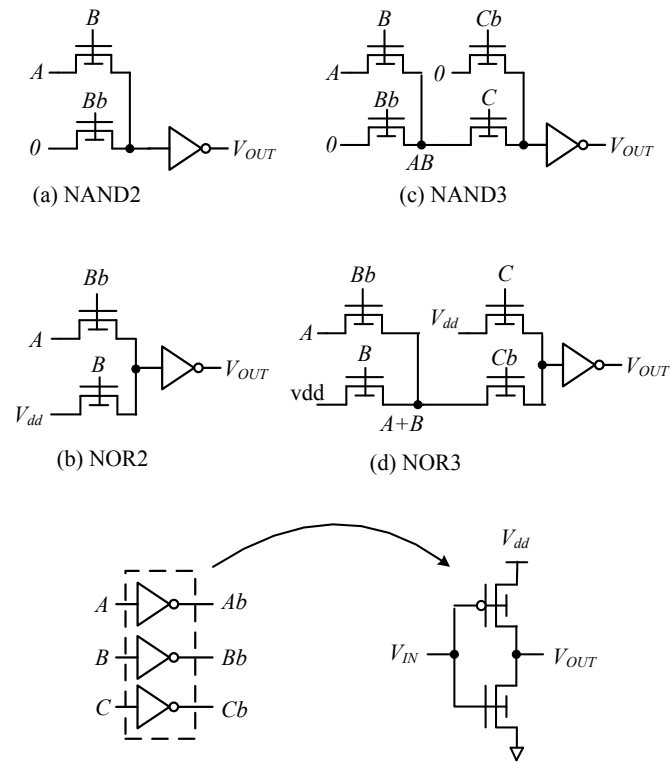


Fig. (5). PTL FinFET gates.

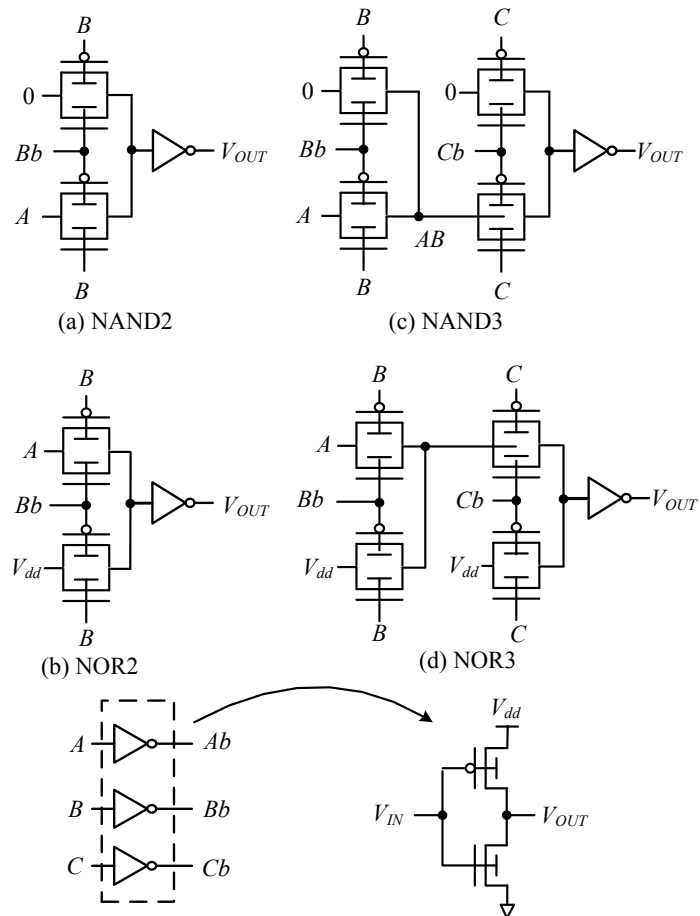


Fig. (6). TG FinFET gates.

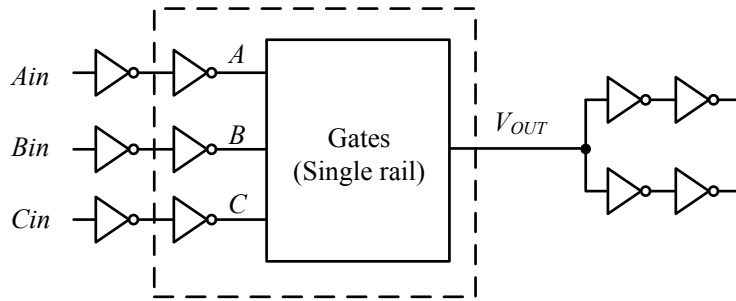


Fig. (7). Test bench of single rail gates for static FinFET logic, TPL, and TG logic.

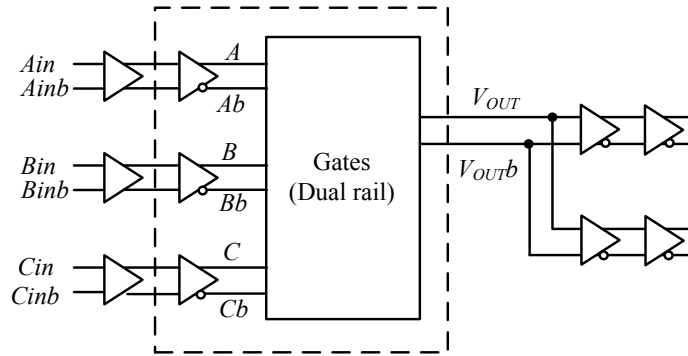


Fig. (8). Test bench of dual rail gates for DCVSL.

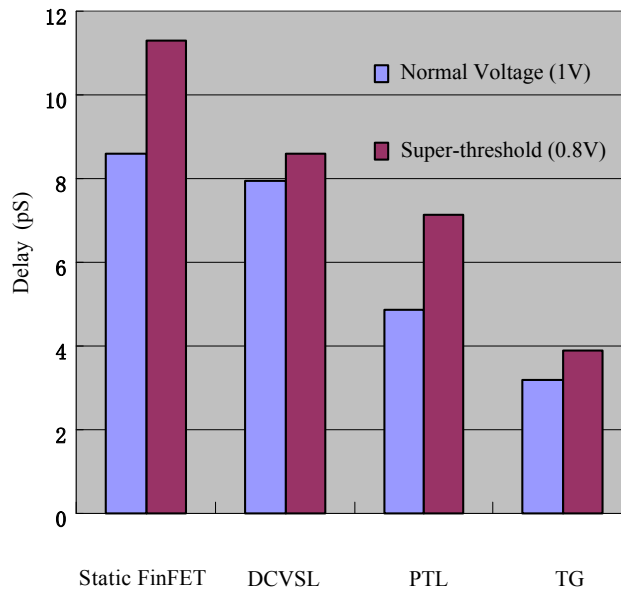
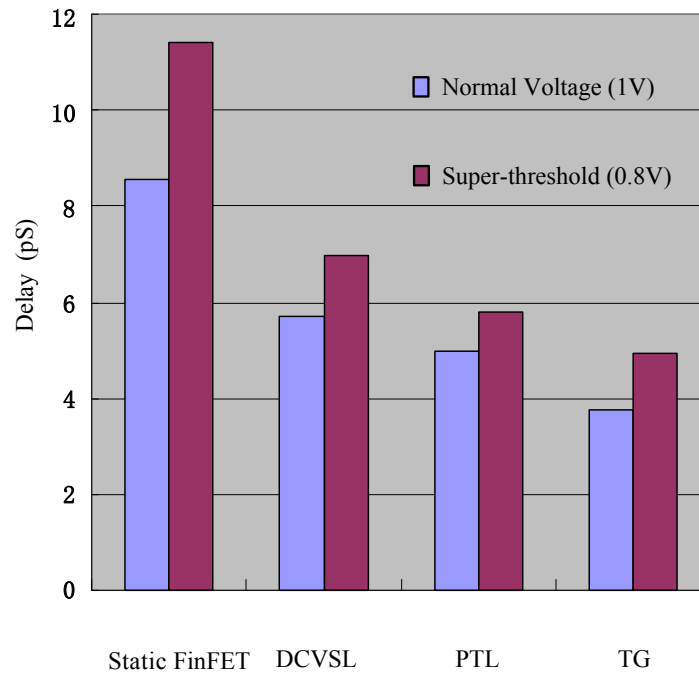


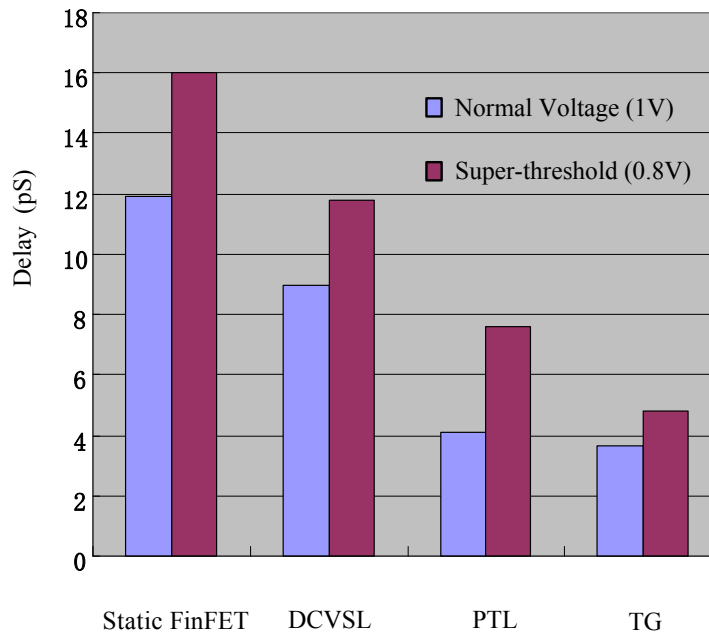
Fig. (9). Propagation delay of the two-input NAND for the various logic styles operating on medium strong inversion regions and strong inversion regions.

where  $t_{pHL}$  and  $t_{pLH}$  are high-to-low and low-to-high output transition time, respectively. The propagation delay of the four gates for various logic styles operating on medium strong inversion regions and strong inversion regions is shown in Figs. (9-12). The normal standard supply voltage of the FinFET circuits is 1.0V. In order to attain favorable performance, the operating voltage in the medium strong inversion regions is taken as 0.8V.

The input gate capacitance is determined by the count of the transistors and their Fin number. The input gate capacitance of the static FinFET is the biggest because of complementary N-type and P-type transistors, while DCVSL and PTL drive only N-type transistors. In addition, the stack height of the static FinFET gate is the largest in all ones. In DCVSL, positive feedback using cross coupled P-type transistors can improve the speed. The stack height



**Fig. (10).** Propagation delay of the two-input NOR for the various logic styles operating on medium strong inversion regions and strong inversion regions.



**Fig. (11).** Propagation delay of the three-input NAND for the various logic styles operating on medium strong inversion regions and strong inversion regions.

of PTL and TG is smaller than DCVSL, resulting in smaller propagation delay. TG has the minimum propagation delay. The static FinFET has 2.9 largest propagation delay as compared to TG logic.

As shown in Figs. (9-13), the delay of FinFET logic gates operating on medium strong inversion regions is only about 23% larger than strong inversion regions. The super-

threshold FinFET circuits show favorable performance. The performance penalty of the super-threshold FinFET circuits differs slightly for various logic families and logic functions.

The power dissipation of the FinFET gates based on various logic styles operating on medium strong inversion regions and strong inversion regions is shown in Figs. (13-16).

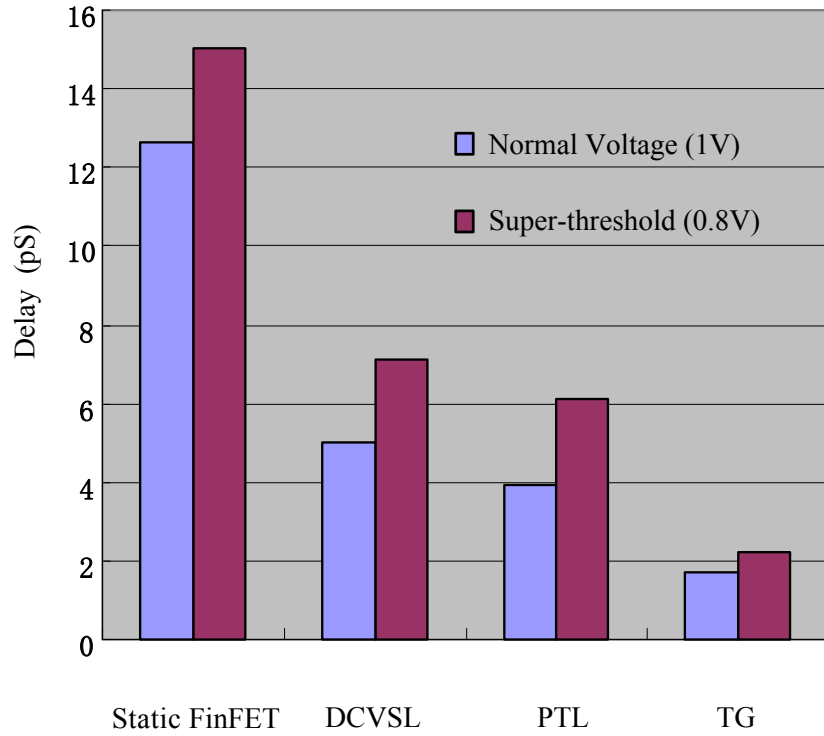


Fig. (12). Propagation delay of the three-input NOR for the various logic styles operating on medium strong inversion regions and strong inversion regions.

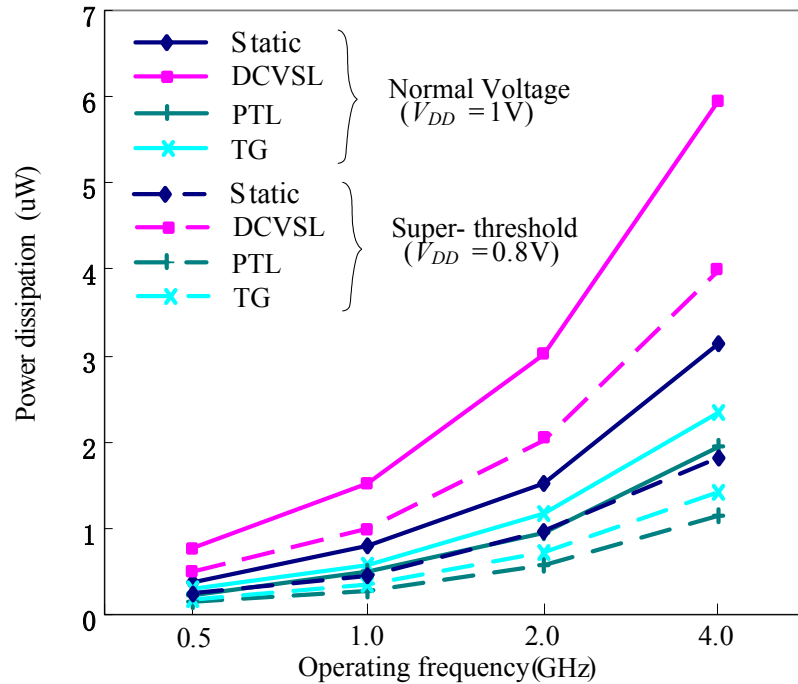


Fig. (13). Power dissipation of the two-input NAND for the various logic styles operating on medium strong inversion regions and strong inversion regions.



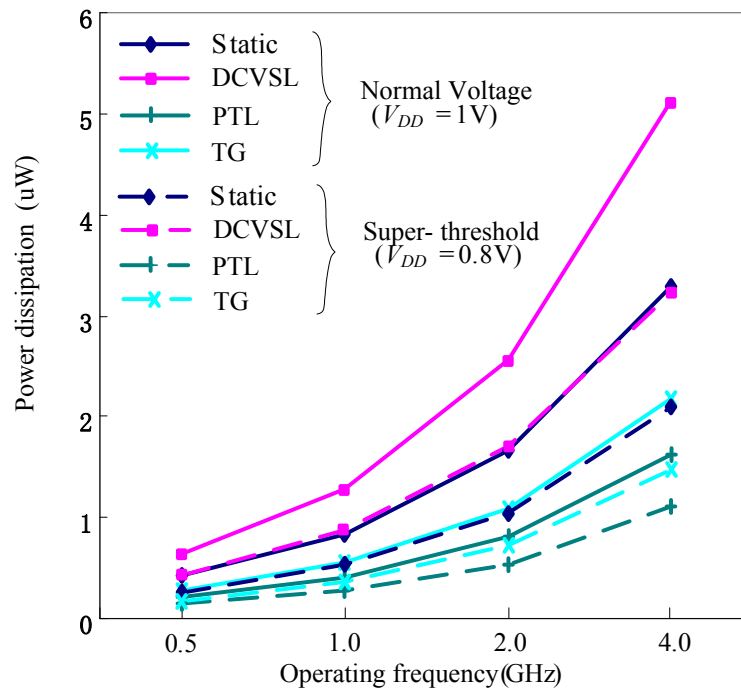


Fig. (14). Power dissipation of the two-input NOR for the various logic styles operating on medium strong inversion regions and strong inversion regions.

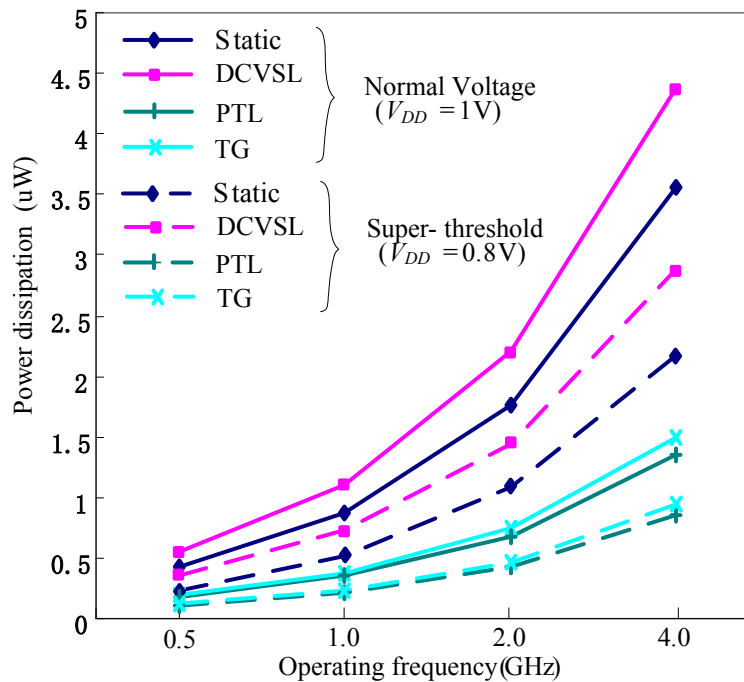


Fig. (15). Power dissipation of the three-input NAND for the various logic styles operating on medium strong inversion regions and strong inversion regions.

The super-threshold FinFET circuits show a great power reduction, compared with normal source voltage.

PTL gates perform the lowest power consumption in all logic families for all operating frequencies. DCVSL gates produce the maximum power consumption because of a

direct-path from supply voltage to the ground during the transition.

As shown in Figs. (13-16), FinFET logic gates operating on medium strong inversion regions attain a power reduction of about 41% as compared to nominal supply voltage

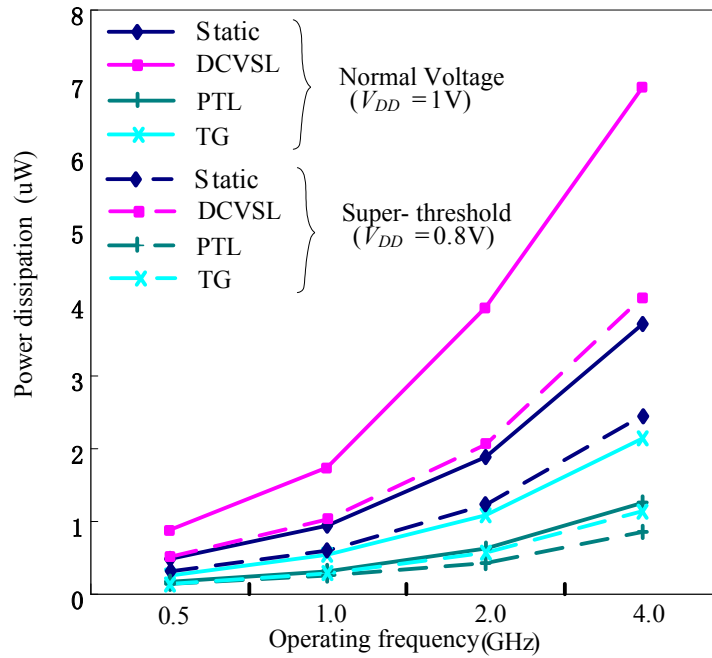


Fig. (16). Power dissipation of the three-input NOR for the various logic styles operating on medium strong inversion regions and strong inversion regions.

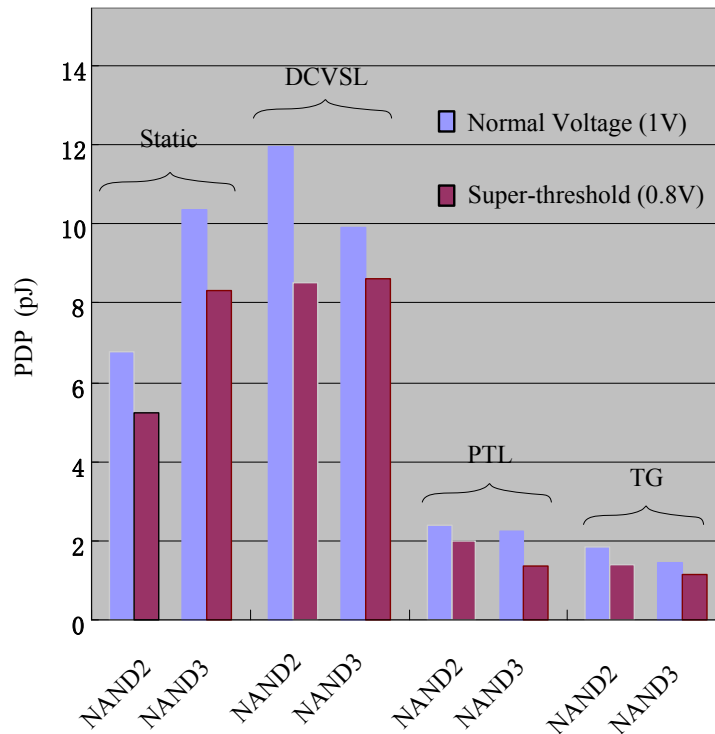


Fig. (17). Power delay product of the two-input and three-input NAND gates for the various logic styles operating on medium strong inversion regions and strong inversion regions at 1.0 GHz.

operation. The power reduction of the super-threshold FinFET circuits differs slightly for various logic families and logic functions.

The power delay product of the two-input and three-input AND gates at 1.0GHz is shown in Fig. (17). TG performs best PDP in all logic families. The three-input AND

gates based on static FinFET, DCVSL, PTL and TG logic operated on medium strong inversion regions provide a PDP reduction of about 23%, 28%, 16% and 24% at 1.0GHz as compared to nominal supply voltage operation, respectively.

## CONCLUSION

Lowering supply voltage of FinFET circuits is an effective way to achieve low power dissipations. The basic FinFET logic gates based on static logic, DCVSL, PTL, and TG logic styles operating on medium strong inversion regions. Strong inversion regions have been investigated in terms of power consumption, delay, and power delay production. The results show that super-threshold FinFET logic gates operating on medium strong inversion regions attain about 41% power reduction with a penalty of only about 23%. The FinFET logic circuits operating on super-threshold regions can attain low power consumption with favorable performance, because FinFET devices can provide better drive strength than bulk CMOS MOSFET.

## CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

## ACKNOWLEDGEMENTS

This work was supported by the Key Program of National Natural Science of China (No. 61131001), National Natural Science Foundation of China (No. 61271137).

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Received: September 16, 2014

Revised: December 23, 2014

Accepted: December 31, 2014

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