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Audio Data Acquisition System Design Based on ARM and DSP

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Abstract: With the rapid development in embedded technology and multimedia technology, digital audio technology has been widely applied. Based on an audio data acquisition system, this paper introduces the communication interface design with respect to the HPl interface between ARM and DSP, and A/D, D/A converter design, and describes the operating principle of interfaces and relevant configuration. A method of audio data acquisition is presented controlled by ARM, with signal processing done by DSP. It provides the system chart of data acquisition and software flow chart. This design scheme can take full advantage of McASP interface to achieve high precision AD & DA converter, and HPl interface has been used to realize high speed data transfer between ARM and DSP, thereby achieving efficient and real-time transmission of huge amount of audio data stream.

Keywords: ARM, Data acquisition, DSP, HPl (host port interface).

1. INTRODUCTION

In the field of audio applications, a large number of operations often require audio data such as acquisition, processing, transmission, storage and other operations at the same time. Only adopting DSP and ARM processor cannot meet the system requirements of real-time and high efficiency, therefore, the combination of ARMS and DSP are used by more embedded real-time application systems to achieve higher performance. Among them, the ARM is the main processor, which is responsible for task management, interface control, and human-computer interaction; whereas, the dependent processor, DSP is responsible for data processing [1]. The high speed data acquisition system consists of ARMS+DSP. The rate of data transmission between ARM and DSP determines the whole performance of the embedded system. Based on fast audio data acquisition system, this paper introduced the data acquisition system design plan of ARM and DSP based on HPI interface, along with the hardware design method and the software flow chart of data acquisition system.

2. THE WHOLE STRUCTURE OF SYSTEM

The S3C2440 micro controller of the ARM9 series of Samsung is used as the ARM processor in this system based on the ARM920T processor, which has the Harvard structure and independent 16 KB instruction Cache and data Cache, along with abundant system resources; the clock frequency can be up to 400 MHz [2]. It is suitable for the application of patterns sensitive to cost and power. The 32-bit high speed floating point TMS320C6713 chip of TI Company is used as the DSP, and the maximum frequency of clock is 300 MHz [3]. The single instruction execution cycle of this system is only 5 ns, with fast processing speed, and it has powerful operational ability with the calculation speed up to 2400 MIPS/1800 MFLOPS [4]. Mainly used for high performance signal processing occasions, the chip can meet the demands of audio algorithm of data processing.

The main functions of the system are to obtain 96 kHz\24 bit high precision sampling rate for real-time acquisition of voice signal, DSP frequency interpolation, digital filtering, processing effect, and real-time playback by D/A conversion. DSP for processing of data uses the HPI interface, and through ARM transmits the data to PC through USB or Ethernet for data analysis, and to understand the working state of the audio signal of the current, the results are analyzed to achieve high quality management. The system is mainly composed of A/D conversion unit, data processing unit, the host communication unit, D/A conversion unit and power supply module; the structure diagram is shown in Fig. (**1**).

3. INTERFACE DESIGNS OF S3C2440 AND TMS320-C6713

In the data acquisition system, ARM as the main processor is mainly responsible for communication control, operating system, calling interface driver, and it can also be used as the storage of a mass of audio data. As the dependent processor, DSP is responsible for the A/D sampling and signal processing and D/A conversion. The communication interfaces between ARM and DSP are mainly dual ports RAM, with serial interface or host interface HPI. The front two ports require additional hardware support, and the HPI methods do not need to increase the peripheral logic circuit, and reduce the hardware cost, which make it very suitable for occasions that require real-time data transmission of large quantity of data [5].

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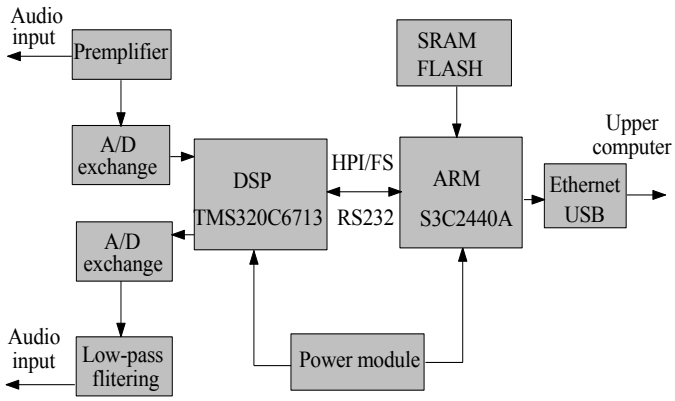

Fig. (1). Data acquisition system structure.

3.1. Introduction on the HPI Interface

The HPI (host port interface) is the 16/32 bit parallel interface specifically signed by TI company to meet the DSP and other microprocessor interface communication, while external host has the control right of the interface. The interface HPI of TMS320C6713 is a 16-bit parallel port. The ARM can directly access the DSP's internal storage space or the address is mapped to the storage space of peripherals through the interface, to achieve DSP resources exchange [6].

HPI of TMS320C6713 completes external communication between the host and DSP through three 32-bit registers as the data registers HPID, the address register HPIA and the control registers HPIC. The HPI interface signal is described in Table **1**. External host and DSP can access HPIC, but only the external host can access HPIA and HPID.

Table 1. Description of HPI interface.

Pin	Function
HD[15:1]	Data bus
HCNTL[1:0]	Access control register
HHWIL	Confirm half word(16bits) input
HAS	Distinguish address and data to reuse address data bus
HR/W	Choice control of read/write
HCS	Chip select signal
HDSI/HDS2	Input data gating
HRDY	Ready signal
HINT	Interrupt signal to host
HWOB	Half word order

3.2. ARM Core Board

The core board is the control and data interaction center of each unit module. This design uses ARM and modules of DSP core boards directly, which is very convenient and saves cost and time. ARM and DSP core boards adopt multi-layer system boards, in which different types are layered and set, which increase the anti-interference ability, reduce common-mode interference, and have high stability. Main pins of two core boards are plugged on the floor in the form of pin for convenient circuit development and debugging.

The ARM core board is composed of the following sections:

CPU: The top portion has S3C2440A processor encapsulated with FBGA;

Storage: Two pieces of 32M SDRAM, and there is one piece of 64M or 128 M flash extension space;

Clock source: Provides 12M system external clock source, 32.768 K RTC clock source;

Power supply: The kernel 1.2V regulates power supply, with the register of voltage regulator module 3.3V.

The core board supports 3.3V and 5V power supply. The bottom has a Samsung 128 MB NAND Flash.

Two pieces of 32M SDARAM have 64 MB memory space After the charging operation, Boot loader copies mirror image document into the corresponding address occupying the space of SDARAM. In this way, an operating system boot software platform is set up.

3.3. The Design of ARM and DSP Interface

ARM micro controller (S3C244) is the main controller. Its external I/O receives the shake hands and interruption request using ARM and DSP software for three registers (HPIA, HPIC and HPID) of the HPI interface respectively, latch ARM from accessing DSP storage unit address, and exchange data. ARM has access of the whole storage space of DSP through addressing the HPI three registers and conducts

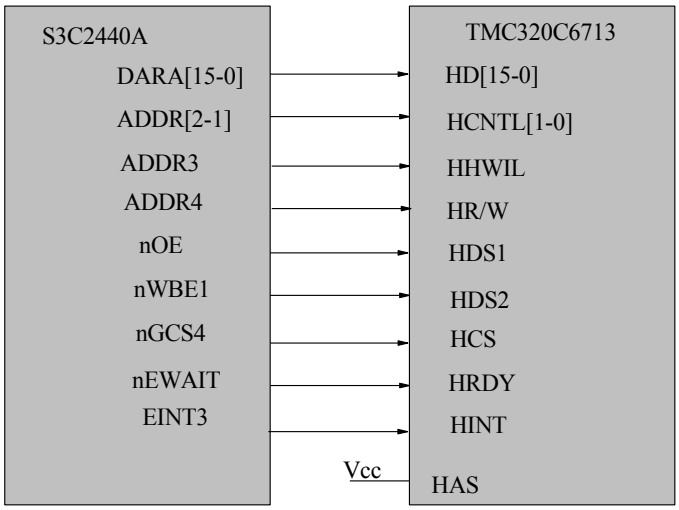

Fig. (2). Data acquisition system structure.

Table 2. Operation choice of HPI register.

HCNTL0	HCNTL1	Function Description
0	0	Host can read and write HPIC.
0	1	Host can read and write HPID, HPIA increase by one after each read operation or decrease by one after each writing operation.
1	0	Host can read and write the HPIA, this register aim at HPI storage.
1	1	Host can read and write HPID, thus HPIA wouldn't be affected

the shake hands communication of DSP. The hardware connection of S3C2440A with TMS320C6713 is shown in Fig. (**2**).

The host operates and chooses to access the HPI registers through HCNTL0 and HCNTL1, these two signal linesas shown in Table **2**. HCNTL1 and HCNTL0 of HPI are connected respectively to the S3C2440 address line ADDR2 and ADDR1. Different registers can be accessed through the operation on ADDR [2:1]. HR/W is read/write input signal for the HPI, when the host drive HR/W=1. the HPI can carry out the read operation; Otherwise, writing operation of HPI is performed [7]. As there is no read/write gating signal of S3C244, therefore ADDR4 is chosen to join the HR/W, which controls the reading and writing states of the HPI through the operation on this address line. HHWII and S3C244 of TMS320C6713 are connected to ADDR3, which are used to identify whether it is the first half word or second half word in the transmission. However, when ADDR3 is zero, it shows the read and write of first half word, and when the ADDR3 is one, it shows the read and write of the second half word. The high half word bytes are determined by the HPIC HWOB [8].

HCS is the Chip Select signal of HPI, which is connected with the selected signal of host nGCS4. The data gating signal is usually comprised of HCS, HDS1and HDS2; the signal is the operation result of the xor between HDS1 and HDS2 and subsequently the nand operation with HAS . HAS is the gating signal address. Due to the S3C244 having independent address and data bus, HAS high level can be fixed. HRDY is connected to the nEWAIT pin of the host to indicate the current state of the HPI access. HINT interrupts signals which are picked up from the external I/O ports on EINT3 of S3C244. HINT is the interruption application that DSP sends to the host, and ARM of the host triggers the interruption of DSP by setting the DSPINT bit in HPIC. Through DSPINT and HINT bits in the HPIC register, the interruption can mediate between ARM and DSP, to coordinate the communication between ARM and DSP.

3.4. FIR Audio Filter

FIR audio filter has been used in this s to collect audio signal. FIR filter has strict linear phase, therefore, the symmetry of filter coefficient should be specially considered; the more the order number of unit impulse, the more storage space is consumed, so the storage space should be arranged and circulation buffer should be used. FIR is usually used in the processing ofvibration signal.

FIR filter is a kind of non-recursive liner system; the difference equation is as follows:

$$y(\mathrm{n}) = \sum_{i=0}^{N-1} a_i x(\mathrm{n}-\mathrm{i}) \quad (1)$$

Its general form is (h(i) is impulse response):

$$y(\mathrm{n}) = \sum_{i=0}^{N-1} h(\mathrm{i}) x(\mathrm{n}-\mathrm{i}) \quad (2)$$

After Z exchange, the system function H(z) of FIR filter can be obtained from the above formula

$$\mathrm{H}(\mathrm{Z}) = \sum_{i=0}^{N-1} h(\mathrm{i}) z^{-1} \quad (3)$$

4. INTRODUCTION OF MCASP INTERFACE

4.1. Overview of McASP

McASP (Multichannel Audio Serial Port) takes the form of time division multiplexing data streams. MCASP uses 12S agreement, and also supports D1T protocol. It has a convenient interface audio equipment to send and receive master clock (AHCLKX, AHCLKR) and mute control (AMUTEIN AMUTE). The serial data lines of MCASP are up to eight roots. Two multichannel audio serials MCASPO and McASPl are integrated on C6713, with these two MCASP reuse external pins with other peripherals on a chip module.

4.2. McASP Characteristics

McASP is the specific audio accessing interface based on DSP of TI Company. It has the following features:

1) Send and receive independent clock;
2) The sending and receiving modules include: Programmable clock and frame synchronization signal generator; 2, 32, 384 of slot TDM data flow; slot which supports 8, 12, 16, 20, 24, 28 bits; the data format bit operation;
3) A total of 16 serial data pins;
4) Can be seamless connected with audio codec, DIR;
5) Compatible with S agreement and supports I2S data format;
6) Integrates the digital audio interface transmitters;
7) When used as DIR receiver, external digital audio interface receiver can be used as the conversion of IIS data format;
8) Performs error checking and correction

5. INTERFACE DESIGN OF A/D AND D/A

McASP (multichannel audio serial port), is a multifunctional synchronous serial interface which is convenient for multichannel audio equipment interface using the 6713 microprocessor. McASP can be configured to a variety of synchronous serial interface standards, which can be directly connected with high-speed interface of all kinds of devices. McASP can send and receive two separate clock generators, and the send and receive can be adopted in different clock frequency; There are total 16 serial data pins; seamless connection can be achieved between McASP and audio ADC, DAC, Codec, digital audio interface receiver DIR and physical device S/PDIF for transmission; multiple IIS data types, and similar data formats can be supported.

DFS is the selection signal for data formatting, the relationship among LRCK, SCLK and SDATA was controlled by DFS pins, in this system, DFS was set high, and serial data output format was set at the I^2S format. S/M was set high, and configured through department pattern; LRCK and SCLK were given as the input. Chip Select CS was set high with the I^2C interface. MCLKA and MCLKD are the simulating alternative selection input clock and digital selection input clock, respectively, and the required frequencies of MCLKA/MCLKD were determined by the output sampling rate.

5.1. A/D part

AD chips adopt CS5396 of CRYSTAL Company, CS5396 uses technology, which can achieve 24 bits high-resolution, and support 96 kHz high sampling rate, and the dynamic range is as high as 120dB. Its input adopts differential structure in order to eliminate noise jamming of common-mode. Data acquisition system composed by CS5396 has the characteristics of high resolution, wide dynamic range, high signal to noise ratio, *etc*. which are especially suitable for the system that needs high precision data acquisition.

The system has two analog input channels, with a piece of CS5396 to implement, working in a controlled way. The work mode can be set up through A/D control ports by TMS320C6713 (sampling rate, master/slave mode, selection of data format, high-pass filtering forbidden, *etc*.).

5.2. D/A Part

D/A chip are adopted with WM8741 in Wolfson Company. WM8741 is a stereo DAC with high performance, which is designed for professional recording system, A/V receiver and the audio application of high-profile CD, DVD and home theater systems.

The length of PCM data input words is supported by the device of 16 to 32 bits, and the sampling rate is as high as 192 kHz. Signal-to-noise ratio is as high as 128 dB, and distortion degree is 100 dB, which is required for a high-performance stereo D/A converter; the high precision digital filter can be directly opened under hardware mode. There are five kinds of digital filters whose response characteristics are set inside, three of which are opened under hardware mode, and other two are controlled by software, which are very suitable for this design.

WM8741 set the control mode of hardware to pull or drop-down the situation in order to determine the working state through specific pins, and the total resistance in the pull or drop-down process was 10kΩ. Settings of WM8741 control pins are shown in Table **3**.

Table 3. Set of WM8741 control pins.

Name of Pin	State	Description
MODE/LRSEL	Pull down	Hardware control module
DIFFHW	Pull down	Hardware control module
OSR/DSDR	High Resistance	96kHz sampling rate state
SCLK/DSD	Pull down	Input is set as the PCM format
DEEMPH	Pull down	Forbidden wiping out strengthen function
IWO/DOUT	Pull up	24 bits I^2S interface set in input end
CSB/SADDR/I^2S	Pull up	24 bits I^2S interface set in input end

5.3. The Design of PCB

The design of PCB (printed circuit board) starts from the principle diagram. The whole designing process is carried out according to the principle diagram; the circuit design tools are Protel DXP 2004 of Altlum Company. The correctness and completeness should be taken into consideration during the designing process of the principle diagram, the label, ports, and to ensure the connection of cables Network bus on electrical connection should be confirmed correctly, and the connection of cross line must be placed by Junction (nodes) to build. Schematic diagram should be readable so that the network label of each unit circuit could be used as much as possible. In the process of designing PCB, the summarization is as follows:

5.3.1. The Layout of the Components

Roughly, structure should be planned at first, such as peripheral interface circuit, serial interface circuit, the general location of the CODEC circuit *etc*., such as ARM and DSP circuits that are generally in two parts, leading to the HPI interface cable in the middle. In this principle, the edge of the PCB components should be more than 2mm from the edge of the plate.

Considering the fixed position of components, the closely related ones should be placed to design the structure , such as sockets, switches, indicator lights, fittings and so on.The LOCK function of the software must be used to lock its position, to avoid the mistaken replacement. Following this, the core components, special components and big components should be placed. Finally, the small devices such as resistors, diodes, and auxiliary small IC should be placed, according to which, unit circuit is affiliated to in the position, function and role of the principle diagram.The layout of its core components is taken to ensure the rationality of the layout, the flow of signal, and the flow of the arrangement of unit function circuit to maintain signal fluency.

Electrolytic capacitor should not be too close to the heat source, in order to avoid premature aging of electrolyte and influence its life. Potentiometer, a toggle switch, which is convenient for adjustment, such as the adjustment inside machine or chassis panel should also be considered in place. Reasonable distinction between analog and digital parts should be considered, to reduce the interference of electromagnetic signals. Noise components such as relay should be far away from the sensitive IC. The layout of the components should not only be uniform and reasonable, but the fluency of the following set should also be considered.

5.3.2. Wiring Components

Because double panel line is used, the two sides of the wires should be kept perpendicular or oblique, to avoid running parallel to the line, and to reduce parasitic FGC. Walk line corner should be kept more than 90 degrees as far as possible, which is best to avoid right angle corner. as , the line length difference is not too big between the address line or cable line,. the length of the signal components should be kept as short as possible; its length should not be more than 2cm. Finally, welding, commissioning, and maintenance convenience should also be considered to obtain the relevant test points for debugging. The ground parts, digital and analog parts should be separated. Low frequency of the circuit should be adapted to single point grounding in parallel; High frequency part, in accordance with the principle of grounding to the nearest should be connected to the multipoint ground. If the ground is thin, the grounding potential changes over current, and lowers the antinomies performance. So the ground should be wide and short , so it can be set up according to the actual situation or copper need to be set, to improve the location problem.

When the layout of line is finished till the end of the text, individual components and layout of line should be adjusted, to check device packaging, DRC, *etc*. The design of whole board PCB is finally completed.

6. THE SOFTWARE DESIGN

The main functions of the software design are to complete data collection, read the data into storage, analyze and process data and output [9, 10]. The software starts the DSP initialization program, provides input analog signal to the A/D converter; starts the A/D converter, sends interruption request signal to DSP after finishing the conversion, turns to

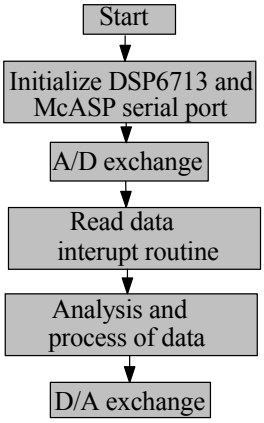

Fig. (3). Flow chart of software.

the interruption service subroutine, reads data, analyses and processes data. The signals after processing are sent to the D/A converter to realize real time audio playback. Software flow chart is shown in Fig. (**3**).

CONCLUSION

Features presented in this paper implemented massive audio data stream for transmission using the HPI interface by controlling ARM. Audio data can be read from external audio and sent to the DSP, or the data through the processing of DSP is sent to ARM through HPI interface. The design of the communication of ARM and DSP is based on HPI interface, as well as the design of 6713 McASP audio interface based on AD, DA interface. This training method can be applied to data acquisition system based on ARM and DSP, which has good practical values. The data acquisition system adopts TMS-320C6713 of TI as the core processor, the S3C2440 of SAMSUNG as the main controller, the TLU320AIC23B of TI as the audio codec, and the system design of double CPU mode makes full use of the fast and efficient calculation speed of DSP and the strong control and human-computer interaction ability of ARM. The HPI interface interconnection is used between DSP and ARM to implement the data exchange between dual-core, the audio acquisition and playback are used to realize TLU320AIC23B technique. A complete set of audio data acquisition system is set up, along with a basic platform for the acquisition and processing of the real time audio signal.

CONFLICT OF INTEREST

The author confirms that this article content has no conflicts of interest.

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